# FLICKER NOISE IN CMOS LC OSCILLATORS

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# FLICKER NOISE IN CMOS LC OSCILLATORS

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For Jennifer, as with everything I do.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| 1/f | Varying inversely with frequency, such as flicker noise |
| $1/f^2$ | 20dB-per-decade phase noise region, or corner to flat region |
| $1/f^3$ | 30dB-per-decade phase noise region, or corner to $1/f^2$ region |
| ADC | Analog-to-Digital Converter |
| AM-FM, AM/FM | Amplitude modulation to Frequency Modulation conversion gain |
| c | Flicker noise slope coefficient |
| CalClk | Calibration clock of the mixed-signal system of Chapter 4 |
| $C_{GS}$ | Gate-source capacitance of a MOSFET |
| CMOS | Complementary Metal Oxide Semiconductor technology |
| $C_{OX}$ | Oxide capacitance of a MOSFET |
| $C_{OX}'$ | Oxide capacitance of a MOSFET per unit area |
| DAC | Digital-to-Analog Converter |
| f | Number of fingers in a MOSFET |
| F | Leeson model excess noise coefficient, >= 1 (unitless) |
| $f_{1/f3}$ | Leeson model $1/f_3$ corner offset frequency |
| $f_C$ | Flicker corner of a MOSFET |
| $f_\Delta$ | Offset from the carrier frequency at which phase noise is measured |
| FOM | Figure of Merit for oscillators |
| $FOM_1$ | Indicative of flicker noise upconversion gain, $FOM_2$-$FOM_3$ |
| $FOM_2$ | The traditional oscillator FOM = $FOM_2$ |
| $FOM_3$ | FOM defined in $1/f^3$ region |
| $g_{gs}$ | Equivalent resistance in induced gate noise equation |
| $g_m$ | MOSFET transconductance |
| GND | Ground, lowest potential in circuit. See also $V_{SS}$. |
| $G_{SS}$ | Equivalent small-signal gain of cross-coupled oscillator |
| IF | Intermediate Frequency |
| ISF | Hajimiri Impulse Sensitivity Function, either Amplitude or Phase |
| $I_{TAIL}$ | Tail current in oscillator |
| k' | $\mu/C_{OX}$ |
| k | Boltzmann's constant, 1.38e-23 J/K |
| K | Flicker noise process-dependent constant |
| L | MOSFET device length, Inductance |
| LC | Inductor-Capacitor |
| LNA | Low Noise Amplifier |
| LSB | Least Significant Bit |
| MIM | Metal-Insulator-Metal capacitor |
| MOSFET | Metal Oxide-Semiconductor Field Effect Transistor |
| NMOS | N-channel MOSFET |
| OTA | Operational Transconductor Amplifier |
| PkN | NMOS peak detector output |
| PkP | PMOS peak detector output |

| | |
|---|---|
| PLL | Phase-Locked Loop |
| PMOS | P-channel MOSFET |
| $P_{OSC}$ | Signal power contained in an oscillatory waveform |
| PSD | Power Spectral Density |
| PSRR | Power Supply Rejection Ratio |
| Q | Quality factor |
| $Q_L$ | Quality factor of an inductor |
| $q_{MAX}$ | Maximum charge stored in tank capacitor (Hajimiri model) |
| $Q_{TANK}$ | Net quality factor of LC tank |
| R(t1,t2) | Autocorrelation function |
| $R_P$ | Equivalent parallel resistance of a tank at resonance |
| *Signal*B | Complementary signal to *Signal* |
| $T_{ng}$ | Effective noise temperature in induced gate noise equation |
| VCO | Voltage Controlled Oscillator |
| $V_{DD}$ | Maximum potential in circuit |
| $V_{DS}$ | Voltage measured from drain to source of a MOSFET |
| $V_{GS}$ | Voltage measured from gate to source of a MOSFET |
| $v_N$ | Voltage below the x-axis in discussion of Chapter 4 |
| $v_P$ | Voltage above the x-axis in discussion of Chapter 4 |
| $V_{SS}$ | Lowest potential in circuit. See also GND. |
| $V_{TH}$ | Threshold voltage of a MOSFET |
| W | MOSFET device width |
| ZIF | Zero Intermediate Frequency transmitter or receiver |
| | |
| $\Gamma$ | Hajimiri Phase Impulse Sensitivity Function. See also ISF. |
| $\Gamma_{RMS}$ | RMS value of Phase ISF. |
| $\Gamma_{DC}$ | DC component of Phase ISF. |
| $\Gamma'$ | ISF multiplied by the periodic normalized current draw |
| $\gamma$ | White noise coefficient |
| $\Lambda$ | Hajimiri Amplitude Impulse Sensitivity Function. See also ISF. |
| $\Lambda_{DC}$ | DC component of the Amplitude ISF |
| $\lambda$ | Channel length modulation parameter = 1/Early voltage•L |
| $\mu_P$ | Mobility of holes |
| $\mu_N$ | Mobility of electrons |
| $\tau$ | Time constant, period of time |
| $\omega_{1/f}$ | Radian flicker noise corner of active devices |
| $\omega_{OSC}$ | Radian frequency of oscillation. |
| $\omega_\Delta$ | Radian offset frequency. See also $f_\Delta$. |

## SUMMARY

Sources of flicker noise generation in the cross-coupled negative resistance oscillator (NMOS, PMOS, and CMOS) are explored. Also, prior and current work in the area of phase noise modeling is reviewed, including the work of Leeson, Hajimiri, Hegazi, and others, seeking the mechanisms by which flicker noise is upconverted.

A Figure of Merit (FOM) methodology suitable to the $1/f^3$ phase noise region is also developed, which allows a new quantity, $FOM_1$, to be defined. $FOM_1$ is proportional to flicker noise upconverted, thus allowing the effectiveness of flicker noise upconversion suppression techniques to be evaluated, despite possibly changing bias points or tank Q, which would change phase noise and FOM in the $1/f^2$ region.

The work of Hajimiri is extended with a simple $\Lambda_{DC}$ estimator for the special case of LC CMOS oscillators. A method of adaptive control of an oscillator core is presented, as well, comprised of a CMOS oscillator with a digitally adjustable N and P width, and a circuit (which is essentially a tracking ADC) which repeatedly adjusts the relative N to P width dependent on the $\Lambda_{DC}$ estimate to maintain the condition of minimum flicker noise upconversion. A fixed calibration constant is sufficient to allow convergence to within 0.7dB of optimal $FOM_1$ for all cases of N width, for a varactorless oscillator test cell.

Finally, a circuit is proposed which would allow the flicker noise reduction technique of cycling to accumulation to be applied to continuous time oscillators, but is not rigorously vetted.

# CHAPTER I

# INTRODUCTION

## 1.1 Flicker Noise in Local Oscillators in Wireless Communications, An Introduction

CMOS implementations of direct conversion receivers (Figure 1.1), the architecture most amenable to complete monolithic integration, are hindered by the $1/f^3$ noise of the local oscillator: an AC-coupled LNA need not contribute any upconverted flicker noise, nor does a passive mixer. Techniques exist (switched capacitor techniques, chopper-stabilized op-amps), however onerous, to provide the required baseband amplification, signal processing, and data conversion, for at least narrow bandwidth signals. What remains without a general solution is the $1/f^3$ noise.

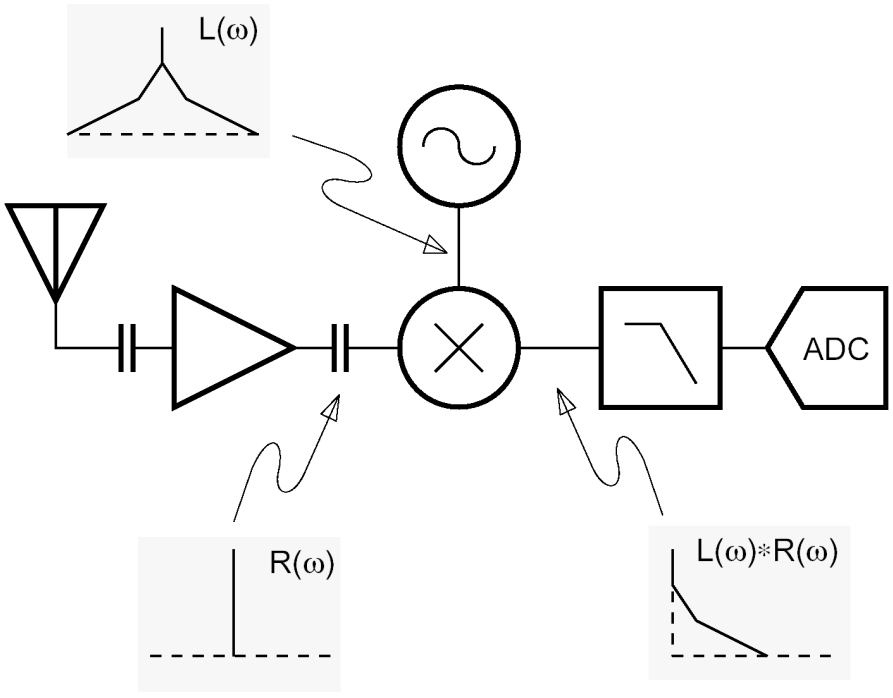



Figure 1.1. Simple Zero IF Receiver Chain.

A multitude of solutions have been proposed, but all lack in either generality or simplicity:

• Low IF architectures [1] have been proposed as an alternative topology which allow for the monolithic integratibility of direct conversion, but also allow the signal to be offset in frequency from the flicker noise and DC offsets. Unfortunately, setting the intermediate frequency to anything but zero also reintroduces an image. Thus, a general low IF solution requires either very accurate quadrature matching (for image reject mixing) and/or protocol complicity (to assure that any image is sufficiently smaller than the desired signal).

• Fractional-N synthesis [2] is often proposed as a general solution to oscillator $1/f^3$ noise, insofar as the frequency raster is independent of the loop bandwidth, and thus the loop bandwidth can be set to a higher frequency than the $1/f^3$ corner of the VCO while still allowing fine frequency resolution. While this is generally correct, it comes at the cost of the complexity of the fractional portion, and the time needed to debug the attendant spur and noise issues.

• Protocols have been proposed (e.g., 802.11*x*) which include no baseband signaling near to DC so as to allow simple methods (i.e., AC coupling) to limit the effect of flicker noise. This requires protocol complicity, and is not usable in systems with narrow (narrow meaning on the order of the flicker corner of the active devices used) channel bandwidths.

• Superior device physics can always be used to this end, but generally at the cost of inferior economics. Bipolar devices have one or more orders of magnitude better flicker corners than CMOS devices, but generally cost more at the same process node.

Thus, a more general approach to understanding flicker noise upconversion in CMOS oscillators has been long sought. The seminal Leeson model is descriptivist in nature, and provides little insight into the underlying upconversion mechanisms. The Hajimiri time variant noise model provides more insight into the upconversion mechanisms, but at the cost of mathematical abstraction. The work of Hegazi and others has described the upconversion pathways in cross-coupled negative resistance oscillators by analogy to switching mixers, with some loss of generality.

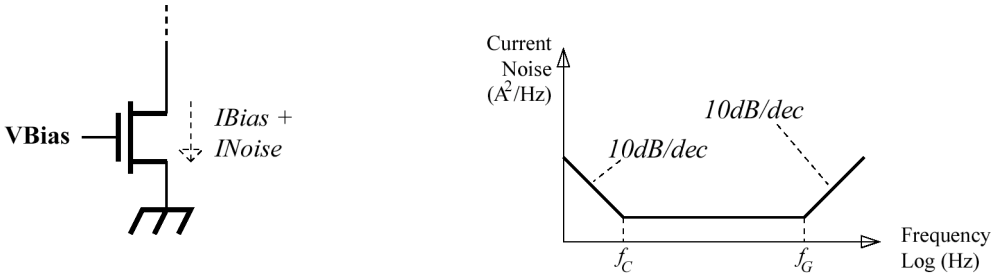
This work will review prior and current work in the area of phase noise modeling, reviewing the work of Leeson, Hajimiri, Hegazi, and others, seeking the mechanisms by which flicker noise is upconverted, and a general method by which the upconversion can be minimized, with particular application to fully integrated CMOS direct conversion receivers, and to cross-coupled negative resistance LC voltage-controlled oscillators. In particular, the work of Hajimiri is extended with a simple $\Lambda_{DC}$ estimator for LC oscillators, and a Figure of Merit (FOM) methodology is proposed for the $1/f^3$ region.

## 1.2 An Overview of Noise in MOSFETs

An N-channel MOSFET, strongly inverted and in saturation, has a drain current which is an ergodic random process, whose time average value is the well-known expression:

$$\bar{I}_{DS} = \frac{k'}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{TH}\right)^2 \cdot (1 + \lambda V_{DS}) \tag{1.1}$$

but which also has a non-zero variance; i.e., noise. Assuming at least wide-sense stationarity for now, the resultant power spectral density (PSD) of this noise process is as Figure 1.2(b).




(a) (b)

Figure 1.2. A single transistor, biased into saturated strong inversion (a), and the resultant PSD (b).

There are three main regions of interest in the spectral plot: the flicker region (a), the white noise region (b), and the induced gate noise region (c). The flicker region, also known as the 1/f or pink noise region, has a spectral density which is inversely proportional to frequency; whereas the white noise region has a flat spectral density. The gate-induced noise region arises from channel noise capacitively coupling to the gate at high frequencies, and thus increases proportionally to frequency.

### 1.2.1 White Noise Region (B)

The white noise region is called such by optical analogy (It has a flat PSD; a light source with similar PSD would look white in color. Exactly why optical analogies are so

popular for noise, this author cannot be certain.); it is also called thermal noise as it arises from the random thermal motion of the silicon lattice (and thus the resultant noise is proportional to temperature).

It can be modeled [3] as a current source connected between drain and source (in a small signal sense, in parallel with the device transconductance) of PSD:

$$\bar{I}_n^2 = 4kT\gamma g_m \quad A^2/Hz \tag{1.2}$$

where:

Table 1.1. Items in white noise equation.

| *Item* | *Value* |
|---|---|
| k | Boltzmann's constant, $1.38 \cdot 10^{-38}$ (J/ºK) |
| T | Temperature (ºK) |
| γ | Coefficient, see below (unitless) |
| $g_m$ | Device transconductance, S |

The coefficient γ is taken as 2/3 for long channel devices. It is suggested [4] that the coefficient may be much larger for short channel devices, but this is not universally accepted. Lee [5] suggests a value of 2-3 for short channel devices.

### 1.2.2 Induced Gate Noise Region (C)

At high frequencies (e.g., a GHz or so), the channel noise is capacitively coupled to the gate, producing a gate noise current. Due to the capacitive coupling, the PSD increases with frequency. For some reason, however, the optical analogy failed to capture the popular imagination here: this noise is never called "light blue" noise.

This noise can be modeled [6] as a noise current between gate and source of PSD:

$$\bar{I}_{ng}^2 = 4kT_{ng}g_{gs} \quad A^2/Hz \tag{1.3}$$

where:

Table 1.2. Items in Induced Gate Noise Equation.

| *Item* | *Value* |
|---|---|
| k | Boltzmann's constant, $1.38 \cdot 10^{-38}$ (J/ºK) |
| $T_{ng}$ | Noise Temperature, where $T_{ng}/T \sim 4/3$ for long channel devices, expected to be higher for short channel devices |
| $g_{gs}$ | $\omega^2 C_{gs}^2/5g_{d0}$ |
| $g_{d0}$ | $V_{ds}$=0 Drain-Source Conductance (S) |

Alternately, induced gate noise may be modeled [5] as a voltage source of white PSD in series with a resistor, in series with the gate capacitance. This alternate model has the advantage of utilizing only white noise sources, at the cost of the complexity of an additional component.

As the gate noise ultimately derives from the channel noise, one might reasonably expect the two noises to be at least partially correlated, and indeed this is the case: the correlation coefficient is found [6] to be 0.395. This potentially allows for at least partial cancellation of this noise [7], if the right clever noise canceling circuit can be discovered.

Finally, it should be noted that induced gate noise is essentially an additive white noise for all but ultra-wideband RF circuits. Consider a 5 GHz VCO with a 1 GHz tuning bandwidth; which would be a very broad tuning VCO indeed. The difference in additional induced gate noise at the top end of the band versus the bottom would be 10*log(5.5/4.5) = 0.87dB, a usually negligibly small amount.

### 1.2.3 Flicker Noise Region (A)

Flicker, also known (predictably) as pink or 1/f noise, is conventionally thought to be caused by traps at the oxide interface, whose time constants are widely distributed depending on the trap depth from the interface [6], but other research [3] has suggested other underlying mechanisms, or perhaps a combination of underlying mechanisms. In any of these cases, flicker noise is modeled as a voltage source in series with the gate, of PSD:

$$\overline{V}_f^2 = \frac{K}{C_{OX}'^n} \cdot \frac{1}{WL} \cdot \frac{1}{f^c} \quad V^2/Hz \tag{1.4}$$

where:

Table 1.3. Items in Flicker Noise Equation.

| *Item* | *Value* |
|---|---|
| K | Process dependent constant. In the case of carrier number fluctuation (i.e., traps), this constant is independent of bias. If mobility fluctuation is posited, it is a function of Vgs. |
| $C'_{OX}$ | Oxide capacitance per unit area |
| n | = 2 in the case of number fluctuation, 1 in the case of mobility fluctuation |
| c | slope coefficient, between 0.7 and 1.2 in the case of number fluctuation, 1 in the case of mobility fluctuation. |

Flicker noise has always intrigued the more philosophical engineer both due to its ubiquity (it is observed in many natural phenomena and informational systems, outside of electronics) and the implied infinite noise power at DC. Flicker noise has been observed in [8][43]:

- The voltages or currents of vacuum tubes, diodes, and transistors
- The resistance of carbon microphones, semiconductors, and metallic thin films
- Average seasonal temperature

- Annual amount of rainfall
- Rate of traffic flow
- The voltage across nerve membranes and synthetic membranes
- The rate of insulin uptake by diabetics
- economic data
- the loudness and pitch of music
- the spectra of most images of the natural world [9]

It was initially suspected that such diversity in systems exhibiting 1/f noise must arise from some fundamental natural law which applies to all nonequilibrium systems [8], but none has been found. More recently [8], flicker noise has been shown to be a nonstationary random process whose autocorrelation function $R(t_2,\tau)$ is a constant versus $\tau$ (for c=1), suggesting flicker noise as a model of or perhaps inherent in human or institutional memory. Finally, given that most images of the natural world have a 1/f spectrum [9], it is not unlikely that preferentially seeking 1/f phenomena would be an evolutionarily selected trait.

The 1/f PSD has always been deemed problematic, for it seems to imply infinite noise power at DC. One approach to this conundrum is to assume at some very low frequency, the noise becomes white or blue, so that the total integrated noise is finite. However, extremely patient research [10] has shown 1/f noise in MOSFETs to extend down to at least $10^{-6.3}$ Hz (1 cycle in three weeks)[1]. An alternate approach by Mandelbrot [11] is to consider 1/f noise as a nonstationary random process; a process whose variance (and thus PSD) varies over time, but observation over a finite time period will always produce finite statistics.

[1] However, correlations cannot be observed over times larger than the total observation time [8]. As the MOSFET has only existed in its modern form since 1960 or so [12], the maximum correlation time which could have possibly been observed is 47 years, or $7 \cdot 10^{-10}$ Hz. Flicker noise is at least bounded in this sense.

Keshner [8][43] clarifies this by analogy to two-dimensional Brownian motion (Figure 1.2). Assuming the particle starts at the origin, and is observed for some time $\tau$, the mean position of the particle remains the origin, but the variance of the particle's position, which is proportional to the square of the radius of the circle in which the particle would be found, increases linearly with $\tau$. If one was insistent on describing this process as stationary, however, and let $\tau \rightarrow \infty$, one would conclude that variance was infinite: the particle could be anywhere in the plane with equal probability. With this mindset, for a finite $\tau$, one would expect that a very large value could possibly occur, but it never would; much as the conventional view of flicker noise.

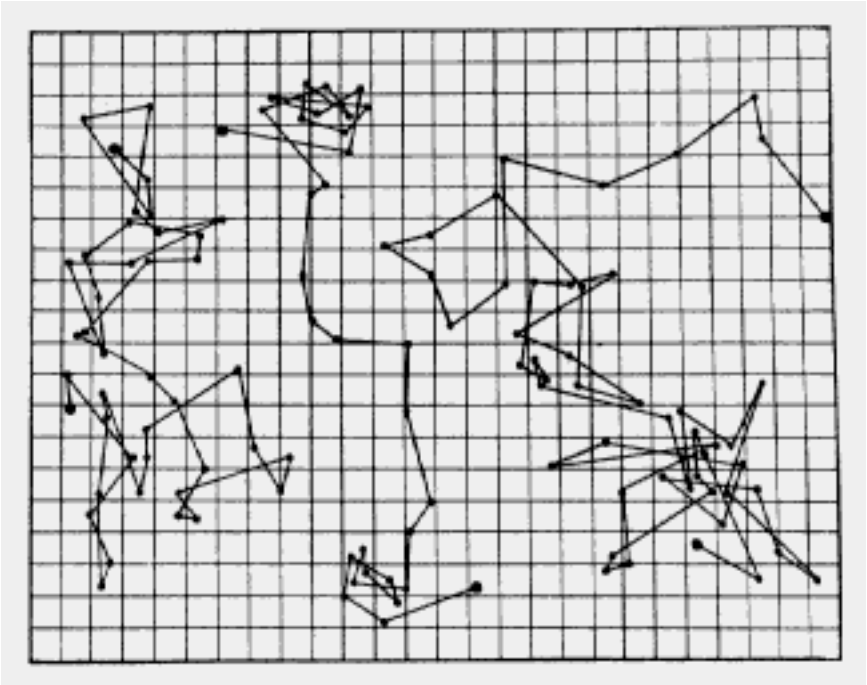


Figure 1.3. Brownian Motion of Colloidal Particles [13].

# CHAPTER II

# APPROACHES TO PHASE NOISE ANALYSIS

## 2.1 Introduction

A ubiquitous desire since the first discovery of oscillators has been to characterize the concomitant phase noise, as a first step towards understanding the sources of this noise and the mechanisms by which they are fitted to sidebands around the carrier. The noise of interest is essentially of two sorts: noise nearby to the frequency of oscillation, whose filtering by the resonator bandwidth to produce 20dB-per-decade noise skirts can be readily understood via a pseudo small signal analysis; and noise near DC (primarily flicker noise) or harmonics of the oscillation frequency, which require frequency conversion mechanisms to produce phase noise near to the oscillation frequency. Figure 2.1 shows the phase noise profile of a typical low-Q CMOS oscillator affected by both sorts of noise: region B demonstrates the 20 dB/decade profile of the first sort of noise;

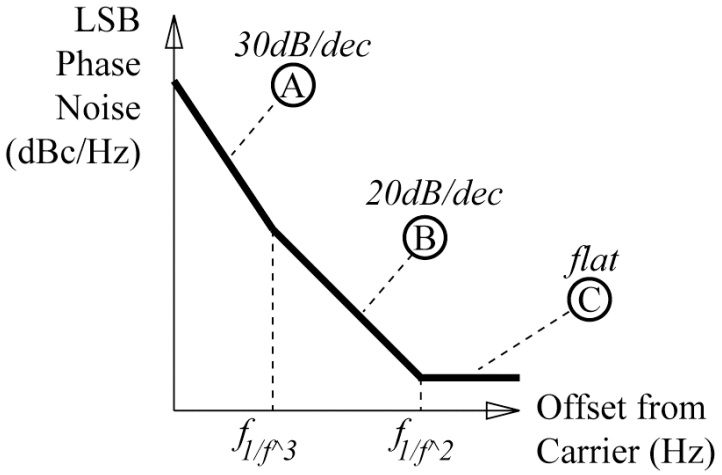



Figure 2.1. Oscillator Phase Noise Profile.

region A is 30 dB/decade due to (frequency translated) flicker noise. The noise floor of region C, although important in some applications (such as the receive band noise of a transmitter), will not be much addressed here. Finally, it should be noted that that Figure 2.1 is not a general phase noise profile for all oscillators (e.g., very high quality factor (i.e., crystal) oscillators might have a resonator bandwidth which is less than the $1/f^3$ corner, which would eliminate region B), but is the general profile of integrated CMOS LC oscillators.

## 2.2 Leeson

Largely considered the seminal work in oscillator phase noise, Leeson's short paper [14] provides an equation with empirical fitting constants which describe regions A, B, and C of the phase noise profile of Figure 2.1 [14],[5]:

$$L_{SSB}(f_\Delta) = 10\log\left\{\frac{2FkT}{P_{osc}}\cdot\left[1+\left(\frac{f_0}{2Qf_\Delta}\right)^2\right]\cdot\left(1+\frac{f_{\frac{1}{f^3}}}{|f_\Delta|}\right)\right\} \qquad (2.1)$$

where:

Table 2.1. Items in Leeson's Equation.

| *Item* | *Value* |
|---|---|
| F | excess noise fitting constant, ≥1 (unitless) |
| k | Boltzmann's constant, $1.38\cdot10^{-38}$ (J/ºK) |
| T | temperature (ºK) |
| $P_{OSC}$ | oscillator output power (W) |
| $f_0$ | frequency of oscillation (Hz) |
| $f_\Delta$ | offset frequency (Hz) |
| $f_{1/f^3}$ | $1/f^3$ corner offset frequency (Hz) |

The resultant topology is as Table 2.2. Note that the phase noise in both regions A and B are proportional to $1/Q^2$ and $1/P_{OSC}$ (and thus to $1/V^2_{OSC}$). This is amenable to intuition: the signal to noise ratio should proportional to the signal level if noise is held constant; and total integrated noise should be proportional to integration bandwidth. The term *F* can be thought of as excess noise; that is, noise in excess of that of the equivalent parallel tank resistance. For a CMOS negative resistance oscillator, F approaches $1+\gamma$ [15], where the channel noise of a MOSFET is $I^2_n = 4kT\gamma g_m$.

Table 2.2. Topology of Leeson's Equation.

| *Feature* | *Value* |
|---|---|
| $1/f^3$ corner | $f_{1/f\text{^}3}$ |
| $1/f^2$ corner | $f_0/2Q$ |
| Noise Floor | $10\cdot\log(2FkT/P_{OSC})$ |

The weaknesses of this approach are readily apparent: as a curve fitting exercise, it provides little insight into the ultimate sources of noise, nor does it provide any details of the nonlinearities at the heart of the $1/f^3$ region; moreover, it predicts infinite noise at the oscillation frequency. Additionally, later work [16],[17] has shown that many details of the Leeson's equation topology are approximate. For example, Leeson claims that the $1/f^3$ corner is identical to the 1/f corner of the oscillator actives. It should be intuitively obvious that such cannot be generally true: two oscillators composed of identical 1/f actives but different upconverting nonlinearities would have different $1/f^3$ corners. Moreover, the $1/f^2$ corner is only approximately as above [5].

Nonetheless, the key insights of the Leeson approach, that (a) phase noise is inversely proportional to $Q^2$, and (b) inversely proportional to $P_{OSC}$, $V^2_{OSC}$, remain immensely valuable and are the underpinnings of later approaches.

### 2.3 Hajimiri Time Variant Noise Model

In contrast to the Leeson's work, the Hajimiri time variant noise model [16],[17], is time domain in nature, and as a consequence provides closer insight into noise upconversion mechanisms. Figure 2.2 illustrates the basic concept of the model: if noise can be considered as a normalized impulse at time $\tau$, the choice of $\tau$ produces varying results. Noise injected at peaks of the single-ended oscillatory waveform (Figure 2.2(a)) modulates the amplitude of the waveform, i.e. induces amplitude noise. Noise injected at zero-crossings of the waveform (Figure 2.2(b)), contrariwise, modulates the zero crossing times, i.e., induces phase noise. The consequences of noise injection at points intermediate between peaks and zero-crossings can be orthogonally decomposed into separate amplitude and phase noise contributions.

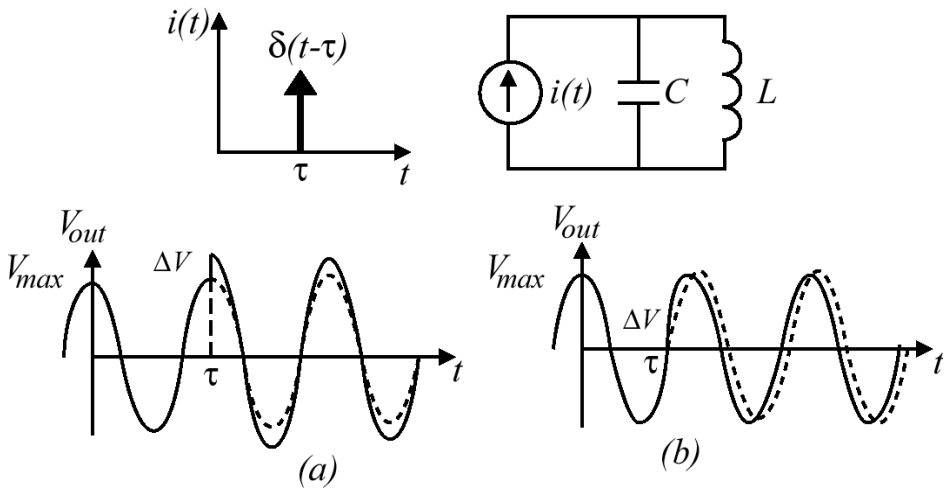



Figure 2.2. Impulse Response of Ideal Oscillator [17].

Amplitude noise is generally more benign than phase noise, for it can be removed by limiting: either the limiting inherent in oscillators themselves, or the limiting that is often designed into post-oscillator amplification to this end. The theory conceives of an Phase Impulse Sensitivity Function (Phase ISF, or, simply, $\Gamma$. The Amplitude ISF is $\Lambda$.), a function periodic in $2\pi$, which indicates the sensitivity of a oscillator waveform at every point in a period to an injected impulse producing a phase shift, as opposed to an amplitude shift. Further, given that noise can only be injected during the portion of a period that the oscillator draws current, the theory further proposes $\Gamma'$, which is the Phase ISF multiplied by the periodic normalized oscillator current draw. Obviously, then, oscillators which only draw current during the peaks of the oscillatory waveform, similar to small conduction angle class C power amplifiers, would excel in this regard. Further work [18] has championed a differential Colpitts topology for its $\Gamma'$ performance.

The net result is as (2.2) [17],[19]:

$$L_{SSB}(f_\Delta) = \begin{matrix} 10\log\left[\frac{\Gamma_{DC}^2}{q_{\max}^2}\cdot\frac{i_n^2/\Delta f}{8f_\Delta^2}\cdot\frac{\omega_{1/f}}{f_\Delta}\right] & \text{Re}\,gion\ A \\ 10\log\left[10\log\left[\frac{\Gamma_{rms}^2}{q_{\max}^2}\cdot\frac{i_n^2/\Delta f}{4f_\Delta^2}\right]\right] & \text{Re}\,gion\ B \end{matrix} \tag{2.2}$$

where:

Table 2.3. Items in the Hajimiri Model.

| *Item* | *Value* |
|---|---|
| $i_n^2/\Delta f$ | noise power spectral density (W/Hz) |
| $\Gamma_{rms}$ | RMS value of $\Gamma$ |
| $\Gamma_{DC}$ | DC ($0^{th}$ order) coefficient of the Fourier transform of $\Gamma$ |
| $q_{max}$ | maximum charge stored in the resonator capacitor (C) |
| $f_\Delta$ | offset frequency (Hz) |
| $\omega_{1/f}$ | flicker corner of the oscillator active devices (Hz) |

Which seems a powerful result: knowing only the Phase ISF and the 1/f corner of the oscillator actives, the $1/f^3$ corner can be predicted (Table 2.4). The devil, however, is in the details: direct computation of the ISF is difficult for most practical oscillators, and is thus most often calculated by direct injection of impulses via simulation or approximate methods [16]. Moreover, there is a chicken-and-egg problem [19]: to design an oscillator to specified performance, the ISF must be known *a priori*. However, given the intimate connection between the time-domain oscillator waveform and the ISF, the calculation of an ISF implies the preexistence of said oscillator. At the very least, a reiterative design approach must be assumed. Finally, it is often difficult to derive clear circuit-level directives from the model: a desire to reduce $\Gamma_{DC}$ in order to improve $1/f^3$ noise may be clear, for example, but exactly what that means in terms of bias current, device size, and so forth, may not be readily apparent for a particular oscillator implementation.

Table 2.4. Topology of the Hajimiri Model.

| *Feature* | *Value* |
|---|---|
| $1/f^3$ corner | $f_{1/f}*(\Gamma_{DC}/\Gamma_{rms})^2$ |
| $1/f^2$ corner | -- |
| Noise Floor | -- |

Nonetheless, the key insights of the Hajimiri model are powerful; both for highlighting the mechanisms of noise conversion, and for its breadth of applicability. Consider the ring oscillator waveforms of Figure 2.3(c): fast rise- and falltimes will minimize $\Gamma_{rms}$, turning the ISF 'spikes' into impulses; and assuring rise- and falltime symmetry will minimize $\Gamma_{DC}$. Further, if this were a CMOS ring oscillator, which only draws current during zero crossings, $\Gamma' \approx \Gamma$, further exacerbating the problem. Studied

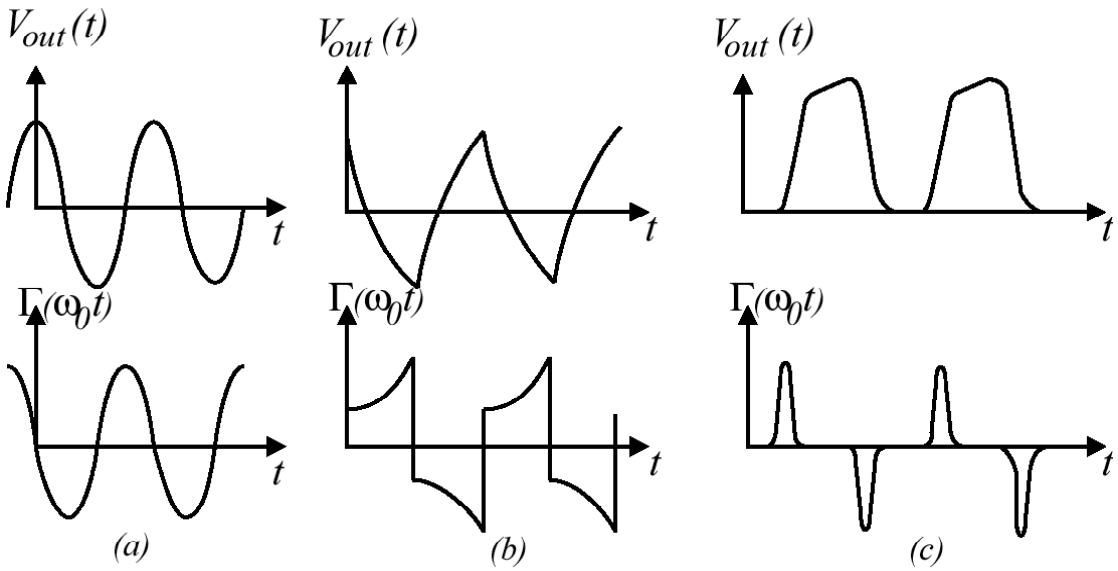



Figure 2.3. Oscillator Waveforms and Associated ISFs: (a) LC, (b) Bose, (c) Ring [17].

familiarity with the Hajimiri model allows a designer to roughly estimate the ISF by eye, and thus have a qualitative estimate of potential improvement to be had, via simple transient simulations. Moreover, the Hajimiri model is generally applicable, so the above is just as true for the prescaler which follows the oscillator, or for any other circuit generally.

Simple orthogonal decomposition of noise impulses into non-interacting phase and amplitude contributions, however, ignores AM-PM and PM-AM effects. Hajimiri's claim

that “neglecting AM-to-PM conversion is not a dominant source of error in prediction of phase-noise in integrated electrical oscillators” [17] may be true for the $1/f^2$ region specifically, or for ring oscillators in general, but is certainly not the case for $1/f^3$ noise in LC oscillators, especially not those with varactors [24].

More elaborate approaches exist [42] which compute directly the AM-PM and PM-AM effects, but generally at the cost of more onerous computation and a reduction in insight. Within the Hajimiri framework, if the amount of amplitude noise converted to phase noise via AM-PM processes is proportional to the total amplitude noise (i.e., if the amplitude noise and AM-PM noise processes are tightly correlated, and the AM-PM noise may be predicted from the amplitude noise via a linear homogeneous estimator; this is a more-or-less common sense view of the world), then minimizing the $\Lambda$ will also minimize the resultant AM-PM noise.

There are also other, less obvious advantages of the Hajimiri model: it is to a large degree complimentary to other approaches. It is largely concerned with the mechanisms of noise injection, rather than the mechanisms of noise generation, which can be dealt with separately; by device sizing, for example. One last subtle strength of the Hajimiri model is that it deals primarily with large signal time-domain phenomena: the self-symmetry of nearly rail-to-rail waveforms. Thus, these phenomena should be readily measurable by in-circuit test measures. Chapter Four discusses one approach to using such measures in an adaptive oscillator to minimize $1/f^3$ noise.

## 2.4 Mixer-Type Analyses

More detailed knowledge of the topology of the oscillator allows for the clearer circuit-level directives that the Hajimiri model lacks, especially with regards to the $1/f^3$ region. This thesis defers a more detailed discussion of the ubiquitous cross-coupled negative resistance oscillator to chapter three, but a minimal topological overview can be sketched here: consider the cross-coupled negative resistance of Figure 2.4 (a) as opposed to the single-balanced mixer of Figure 2.4 (b). In the presence of a large-signal oscillation, the cross-coupled pair, in addition to its small signal function, will obviously also have a large-signal commutating mixer action. Ignoring parasitic capacitances, Figure 2.4 (a) will have similar upconversion gain for baseband signals as Figure 2.4 (b), which was specifically designed to that end. This is obviously problematic.

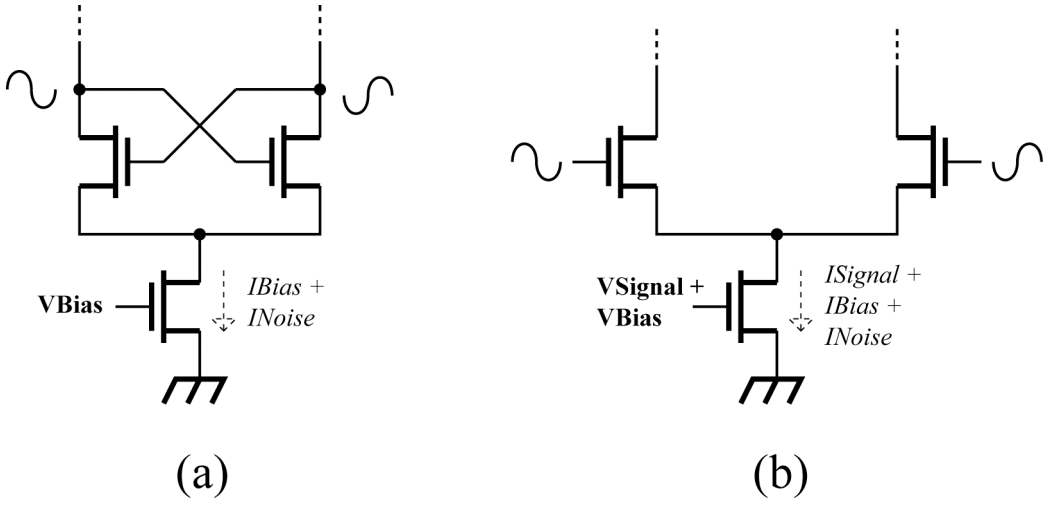



Figure 2.4. Similar Topologies: (a) Negative Resistance Oscillator, (b) Single Balanced Mixer.

Hegazi and others [15], [20]-[24] clarify these mixer-like mechanisms at the heart of the $1/f^3$ region. The baseband noise upconverted in this manner becomes AM sidebands around the carrier, and requires an AM-FM mechanism to become phase noise. The voltage-dependent capacitance of the varactor is generally the dominant mechanism [22]. Moreover, mismatch and other mechanisms can result in noise upconversion to twice the oscillation frequency [15]. Although the resonator will filter the twice-frequency component to some extent, the unfiltered remainder will then be downconverted to phase noise sidebands around the carrier.

The key insights of the mixer-type analyses, then, are to consider the oscillator system in the frequency domain, and to eliminate any unnecessary spectral components. Traps to block second harmonic currents in the current tail have been shown to improve flicker noise, and phase noise generally [15]. Others have eliminated the current tail and its concomitant noise entirely [24]. Minimization of varactor AM/FM, as technology allows, will substantially improve flicker noise [22].

### 2.5 Figure Of Merit (FOM)

A method of comparing oscillators with a single number has long been desired. A spot phase noise number is difficult to compare, unless at the same offset and the same carrier frequency. And even then, variation in the supply voltage allows for tradeoffs between consumed power and phase noise. A commonly used figure of merit (FOM) for integrated oscillators, which takes into account all of these factors, is:

$$FOM_2 = L_{SSB}(f_\Delta) + 20\log\left(\frac{f_\Delta}{f_0}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \tag{2.3}$$

This FOM is used ($f_\Delta$ is chosen such that it is) in the $1/f^2$ region, and the $1/f^3$ corner is taken as its lower bound of applicability. Although the $1/f^3$ corner is not, per se, a useful indicator of total frequency converted noise (for the $1/f^3$ corner can be reduced to any desired frequency by making the $1/f^2$ region more noisy; by putting a flicker-noise-free resistor across the tank, for example), the above FOM in conjunction with the $1/f^3$ corner is. However, a single number metric can also be defined. If the above FOM is specifically defined to be in the $1/f^2$ region and called $FOM_2$; and a second FOM, defined in the $1/f^3$ region, is called $FOM_3$ (2.4); then a third quantity can be defined, $FOM_1$ (2.5), which is indicative of total frequency converted noise. This useful result will be put to use in Chapter Four.

$$FOM_3 = L_{SSB}(f_\Delta) + 30\log\left(\frac{f_\Delta}{f_0}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \tag{2.4}$$

$$FOM_1 = FOM_2 - FOM_3 \tag{2.5}$$

## 2.6 Conclusions

The multiplicity of phase noise analysis approaches are in many ways complementary. A designer might think of them in composite as the Venn diagram of Figure 2.5: a designer in the nascent stages of a design would primarily consider the Leeson model, selecting tank Q and biasing actives to produce the required swing. As the design matures, the greater sophistication of the Hajimiri and Mixer-type approaches allows greater tradeoffs, especially in the $1/f^3$ region.

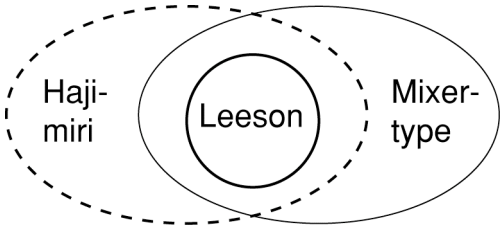



Figure 2.5. Relationship among Phase Noise Analysis Approaches.

# CHAPTER III

# DETAILS OF THE CROSS-COUPLED NEGATIVE RESISTANCE OSCILLATOR CORE

## 3.1 Introduction

The cross-coupled negative resistance oscillator [1] is a triumph of simplicity and (thus) ubiquity. Its simplicity is such that even the greenest of engineers can have modest hopes of achieving within 20 dB of best-in-class Figure Of Merit when hooking together its handful of transistors, an inductor, and tuning capacitance. Wringing out that remaining 20dB, however, has underwritten a generation of academics [25], [26].

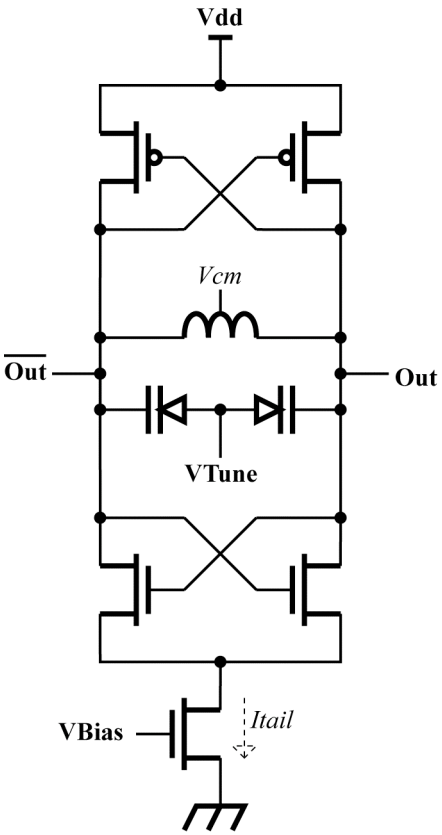



Figure 3.1. Prototypical Cross-Coupled Negative Resistance Oscillator.

The basic prototype of such an oscillator is as Figure 3.1. Assuming $g_{mN} = g_{mP} = g_m$, the net differential resistance of the cross-coupled N- and PMOS pairs is $-2/g_{mN} \mid -2/g_{mP} = -1/g_m$. The current tail sets the bias point, which in turn sets the oscillation amplitude, and thus phase noise. The inductor in conjunction with the varactor and parasitic capacitances sets the frequency of oscillation, $\omega_{OSC} \approx 1/\sqrt{LC}$. Many variations from this basic topology are possible, but these properties are common.

## 3.2 Aspects of VCO Design

### 3.2.1 Minimum $g_m$ Required for Oscillation

If the equivalent parallel resistance of the LC resonator is $R_P$, then the minimum negative resistance needed to guarantee oscillation in a small signal sense is $-R_P$. Thus, for an NMOS or PMOS only oscillator, $g_m \geq 2R_P$; for a complementary N and P oscillator, $g_m \geq R_P$. In practice, a somewhat smaller resistance magnitude is required; to assure that the oscillation amplitude will grow to the bounds of the limiter action; as well as assuring startup over variations in process, temperature, and voltage; and to minimize startup time.

By analogy to the Barkhausen criterion [27], a 'small signal gain' can be defined [28] to be ($g_{mN} = g_{mP} = g_m$) $G_{SS} = g_m R_P$ for complementary oscillators, and $g_m R_P/2$ for NMOS or PMOS only oscillators. A historic design recommendation, given without formal justification, has been to set the nominal 'excess gain' to $G_{SS} = 3$. The thought was that the excess gain should be set to the minimum required for reliable startup, for more gain than absolutely necessary would worsen phase noise. This seems amenable to small-signal intuition: more amplification of the noise of $R_P$ should make phase noise worse.

In modern integrated practice, simulation over process, voltage, and temperature corners will indicate the minimum $G_{SS}$ required to guarantee startup, but this is often quite close to the historic recommendation [31].

### 3.2.2 Specification of Bias Current

From a bias current selection point-of-view, there are two regimes of operation for the cross-coupled negative resistance oscillator: current limited and voltage limited [25]. In the current-limited regime, the oscillator output amplitude is proportional to bias current, and will increase linearly with current until reaching the limits of the supply rails, and thus entering the voltage limited regime. Specifically, in the current-limited regime, the fundamental amplitude of the differential output is $(4/\pi)I_{TAIL}R_P$ if square-wave switching of the current can be assumed (i.e., at low frequencies), reducing to = $I_{TAIL}R_P$ at high frequencies, where the current waveform looks more sinusoidal due to a more finite $f_{OSC}/f_T$ [25]. As per the Leeson model, phase noise at a given offset is proportional to $1/V^2$, and thus proportional to $1/I_{TAIL}^2$, in the current-limited regime.

From a circuit point-of-view, as the circuit goes deeper into the voltage-limited regime, the cross-coupled pairs will spend a greater portion of the waveform period in triode. As the $r_{DS}$ of the active devices is reduced in triode, it should be expected that the phase noise will degrade in the voltage-limited regime. As shown in Figure 3.2, this is indeed the case: a phase noise maxima can be seen at the transition from current to voltage limitation. The broadness of the maxima is a result of both the incrementalism of the mechanism and because the amplitude of oscillation continues to increase somewhat

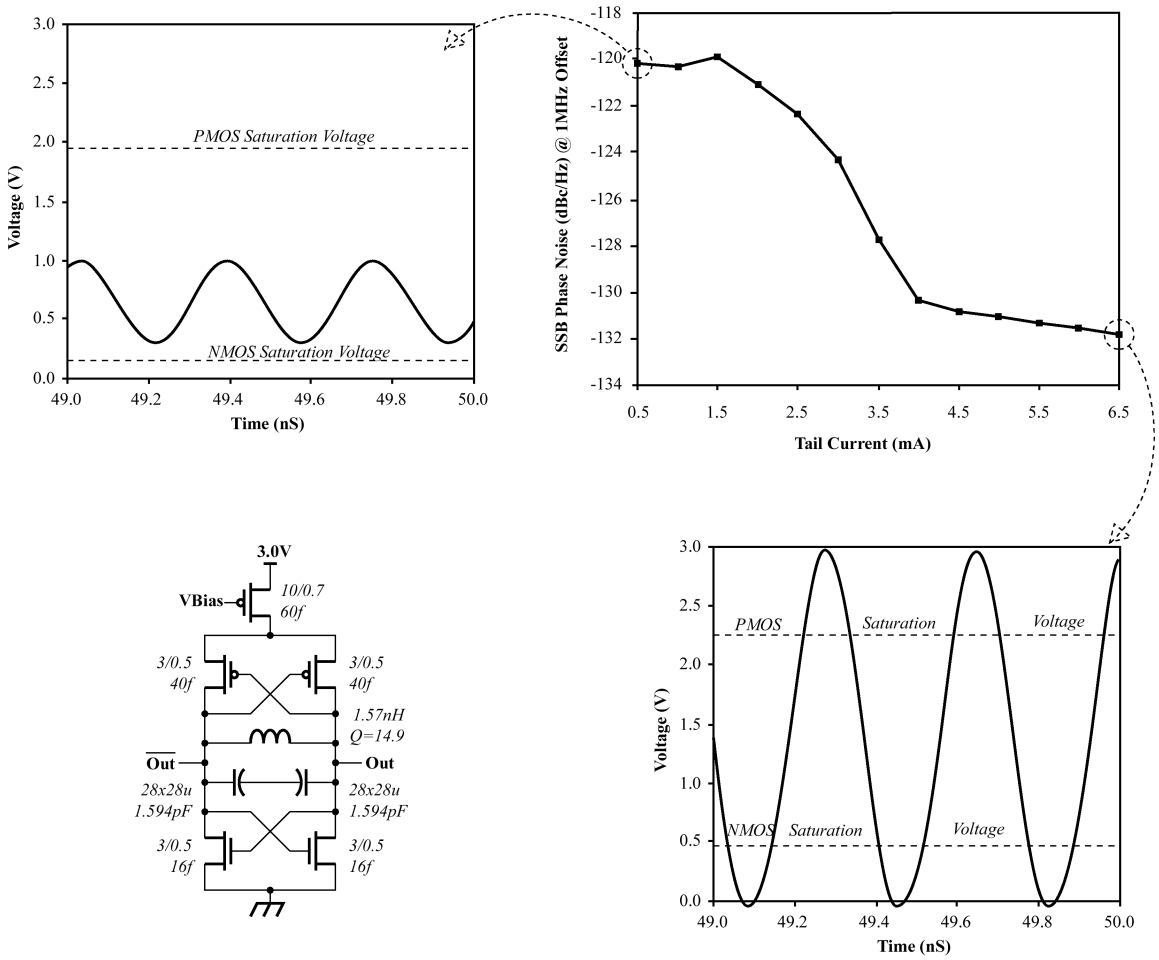



Figure 3.2. Simulated Phase Noise at 1 MHz Offset Versus Bias Current ($f_{OSC}$=2.7 GHz; Jazz 0.35μm BiCMOS process, using only CMOS devices).

as the oscillator is pushed further into voltage-limitation and thus blunt the effect of the reducing tank Q.

If the design goal is to maximize phase noise, then the bias current is constrained to this transition. If the design goal is to maximize FOM, then somewhat more freedom to select the bias point is allowed. An interesting aspect of MOS oscillators is that even if the bias current is taken as constrained, the $g_m$ of the oscillator core can be separately optimized via device sizing.

### 3.2.3 Frequency of Oscillation

The frequency of oscillation may be estimated as being the same as the small-signal resonant frequency of the LC tank in isolation:

$$f_R = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

where the $L$ is explicit, and the $C$ consists of fixed capacitance, variable capacitance determined by the tuning voltage, and parasitics. For coarse estimates, this is accurate enough, but error terms must be considered if finer resolution is desired.

It is noted [26],[29] that, in the typical case of nearly rail-to-rail oscillatory waveforms, the instantaneous bias voltage across the varactors are a function of $V_{Tune}$, the oscillator output common mode voltage (assuming the varactors are DC coupled to the output nodes, as per Figure 3.1; the varactors could be AC coupled, of course.), and the instantaneous waveform voltage. The net effect is that the instantaneous varactor capacitance, and thus oscillation frequency, is a function of the oscillation amplitude. In

the limit case of a step in capacitance from $C_{MAX}$ to $C_{MIN}$ at varactor bias voltage V′, the tuning gain can be approximated as [29]:

$$K_{VCO} \cong \frac{\omega_H - \omega_L}{A_0} \quad (rad/s/V) \tag{3.2}$$

[6]

Where $\omega_H$ and $\omega_L$ are maximum and minimum frequencies of oscillation, which correspond to the oscillatory waveform being entirely above or below V′ (and thus the varactor presenting a constant $C_{MIN}$ or $C_{MAX}$, respectively), and $A_0$ is the oscillation amplitude.

The above is also a flicker noise upconversion mechanism, complementary to varactor AM-PM: that is, that the oscillation frequency is a function of oscillation amplitude, which is a function of bias current, and thus flicker noise upconverts. Separately, modulation of the output common mode voltage [24] (assuming the varactors are DC coupled) can also provide an upconversion pathway. Excessive harmonic content [30] and nonidealities in the amplitude limiting process are also sources of frequency variation.

### 3.2.4 Maximize L or Maximize C?

Another historic design recommendation, also given without formal justification, has been that maximizing the inductance in an oscillator (which has the obvious consequence of minimizing the capacitance, for a given frequency of oscillation) will improve phase noise. This author assumes the following chain of assumptions drove this recommendation: (1) the quality factor of the capacitors used in oscillators was

historically (and still generally is, both in integrated and discrete contexts) much higher than that of the inductor, so $Q_{TANK} \approx Q_L$, (2) the frequency of oscillation was much smaller than the frequency of peak $Q_L$ ($fQ_L \approx ½ \bullet$ self resonant frequency), (3) so increasing the inductance value, which will reduce the frequency of peak $Q_L$, will increase $Q_{TANK}$.

The validity of some of these assumptions in a modern integrated context is obviously suspect: although $Q_{TANK}$ remains approximately equal to $Q_L$, frequencies of oscillation can be close to or even higher than the frequency of peak $Q_L$. Moreover, inductors in an integrated context are generally of lower Q, which lessens the payoff of such optimization efforts. Finally, the reduced $Q_L$ in conjunction with the many degrees of freedom in inductor design in an integrated context make it so that widely varying inductance values can be crafted with the same $Q_L$ at any frequency of interest.

The limit case of 'White $Q_L$' (that is to say, $Q_L$ is nearly constant across all inductance values of potential interest to a particular oscillator design) is an interesting one: recent work [31] has suggested minimizing L to minimize phase noise in such a case. Practical considerations (i.e., unextracted interconnect inductance becomes a dominant contributor to the total net inductance as the explicit inductance approaches zero, making the oscillation frequency difficult to predict) limit the extent to which this directive can be taken. Of course, other objectives could justify a more moderate L/C ratio: as the current required to achieve a specified voltage swing is determined by the equivalent parallel tank resistance, $R_P$, and:

$$R_P = Q\sqrt{\frac{L}{C}} \tag{3.3}$$

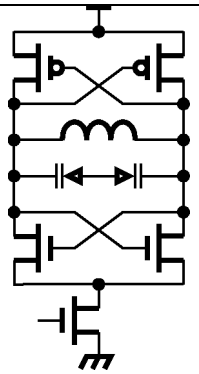
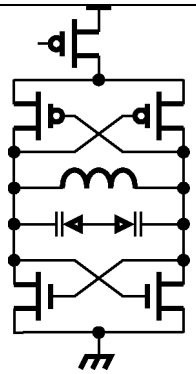
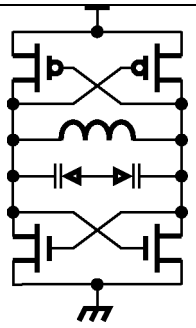
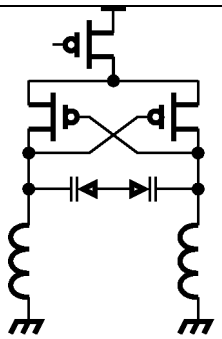
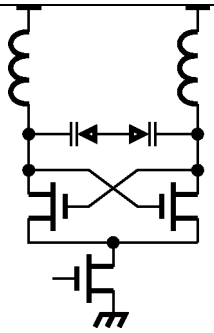
Thus, if $Q_{TANK} = Q_L$ = constant, the current required for the specified swing is entirely determined by the L/C ratio (the square root of the L/C ratio is often called the characteristic impedance, in analogy to distributed circuits). Thus, a FOM target may specify a tank characteristic impedance.

### 3.2.5 Variations on a Theme

A representative subset of the nearly infinite possible variations on the cross-coupled negative resistance oscillator theme is shown in Table 3.1: the cross-coupled pair may be NMOS, PMOS, or both. The current tail may be NMOS, PMOS, or non-existent. The complementary topology is often chosen if minimizing flicker noise is desired: an optimally sized design can counter an NMOS "push" with an equal and opposite PMOS "pull" and maximize single-ended output waveform self-symmetry, thus minimizing the DC component of the Hajimiri ISF. On the other hand, the maximum differential swing of a complementary core is somewhat less than $2 \bullet V_{DD}$; whereas a non-complementary core can swing nearly $4 \bullet V_{DD}$. Per Leeson's equation, this should represent a 6dB improvement in phase noise, all other things being equal.

The current tails can be either N- or PMOS, or neither: for both the current tails and cross-coupled devices, P- devices are preferred for their lower flicker corners, whereas N-devices have higher $f_T$s. In addition to setting the bias current, the common mode impedance of the tail also affects PSRR [29]. Unfortunately, the current tail also

Table 3.1. Some Possible Variations on the Cross-Coupled Negative Resistance Oscillator.

| | Bottom Tail | Top Tail | No Tail |
|---|---|---|---|
| CMOS |  |  |  |
| PMOS | |  | |
| NMOS |  | | |

contributes a large amount of noise, and flicker noise in particular, while contributing nothing to the essential function of the oscillator. Designs without explicit current tails [29],[32] are generally biased well into the voltage limited regime, for the bias point is not explicitly established, and thus will vary with process, voltage, and temperature variations. This will cause the oscillatory amplitude and thus phase noise to vary widely with PVT, unless the oscillator is severely voltage limited. Even with such aggressive voltage limiting, tail-less designs generally have superior phase noise performance to similar designs in the same technology with tails [29],[32].

It should be noted that while the $2 \bullet V_{DD}$ maximum single-ended swing of the bottom-tail NMOS core is fairly benign (hot electron effects and other reliability issues aside), being from $V_{SS}$ to $2 \bullet V_{DD}$, the top-tail PMOS core swings a full $V_{DD}$ below $V_{SS}$. If, as is normal practice, the substrate is at the $V_{SS}$ potential, this severely risks latchup. Thus, the top-tail PMOS topology should be approached with caution. Additionally, at multi-gigahertz frequencies, scaling a $2 \bullet V_{DD}$ single-ended swing to something less than $V_{DD}$ in order to drive the next stage, while retaining the phase noise performance, can be surprisingly difficult: MIMs have voltage limitations, and metal-metal capacitors are often of low Q at such frequencies.

### 3.3 Strategies Against and Mechanisms of Flicker Noise Upconversion

Essentially, there are two meta-strategies towards minimizing flicker noise in CMOS LC VCOs: (a) minimize flicker noise upconversion mechanisms, and (b) minimize flicker noise generation. The lion's share of chapter two of this thesis can be applied towards the first strategy: maximizing Q and swing, maximizing waveform single-ended self-

symmetry, and minimizing varactor AM-FM and second harmonic current can all do their part to minimize upconversion. Flicker noise generation can be minimized by increasing the WL product of the cross-coupled pair(s) and tail, and eliminating the tail, if possible. Additionally, the method of section 3.4, below, can also be applied to this end.

### 3.4 Cycling to Accumulation: A Method to Reduce Flicker Noise Generation

It has been shown [33],[34] that periodically cycling a MOSFET from strong inversion (normal mode of operation) to accumulation (reset) (i.e., periodically reducing $V_{GS}$ from its normal value to zero) will reduce flicker noise while in strong inversion, for those frequencies less than or equal to 1/cycle period. It is thought that oxide interface trapping/detrapping is the dominant source of flicker noise; this technique is thought [33] to empty all oxide interface traps of time constants less than the cycle period.

This technique has been exploited in sawtooth [35] and ring oscillators, which are naturally switching from rail to rail. Application to LC VCOs is somewhat more problematic: a requirement for continuous operation precludes setting $V_{GS}$=0 for the entire oscillator core. A topology that might work for continuous LC oscillators is shown in Figure 3.3: the cross-coupled pair of width nW is divided into n fingers of W

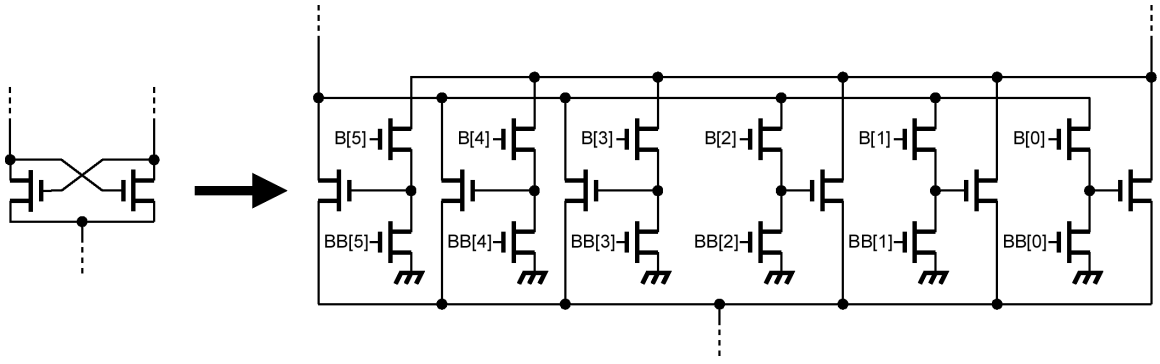



Figure 3.3. A Topology for Cycling to Accumulation for Continuous Time LC Oscillators.

width. By virtue of this segmentation, the active core may be cycled to accumulation in parts, allowing the strongly inverted remainder to maintain the oscillation.

For example, suppose the design of Figure 3.3 requires 2 fingers for both devices in normal operation. If so, then one finger can always be ‘reset’ while leaving two fingers in ‘normal operation’ mode, maintainng the oscillation. If this procedure is continuously performed with a reset clock of frequency *f* and duty cycle *d*, then the frequency of resetting any one finger is f/n, and the reset duty cycle for any one finger is d/n. The reduction in flicker noise amplitude was found [33] to be nearly independent of reset duty cycle.

# CHAPTER IV

# A SIMPLE ESTIMATOR FOR $\Lambda_{DC}$ FOR THE SUBSET OF WAVEFORMS FOUND IN LC VCOS

## 4.1 Introduction

The greater portion of Hajimiri's thesis [16], [17] contemplates ring oscillators, which support what can be considered, from a $\Lambda_{DC}$ perspective, to be a superset of the waveforms present in LC oscillators. The harmonic filtering inherent in LC oscillators constrains the possible output waveforms: for example, in the limit case of infinite loaded Q, asymmetric rise- and falltimes are not possible. A simple estimator for $\Lambda_{DC}$, as will be shown below, can be built for the subset of oscillatory waveforms with symmetric rise- and falltimes.

As previously shown, AM-FM distortion arising from non-linear capacitances in varactors and active devices is a dominant source of single-ended waveform asymmetry [24] in LC oscillators. Consider the piecewise continuous output waveform of Figure 4.2 to be a model of the AM-FM distortion of [24, reproduced below as Figure 4.1], where:

$$\begin{aligned} &I)\ V(t) = -A_0 \sin(\omega_1 t) \quad 0 \le \phi < \pi \\ &II)\ V(t) = -A_0 \sin(\omega_2 t) \quad \pi \le \phi < 2\pi \\ &\omega_1 > \omega_2 \end{aligned} \tag{4.1}$$

Then the Amplitude ISF for each half period would be [16][2]:

[2] See Appendices A and B for a detailed development of the ISFs.

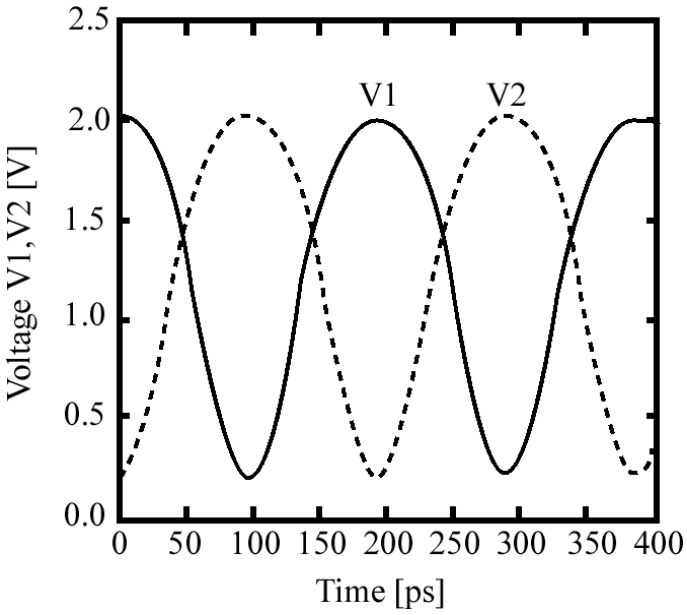



Figure 4.1. AM-FM Distortion Effects on Single-Ended LC Oscillator Waveforms [24].

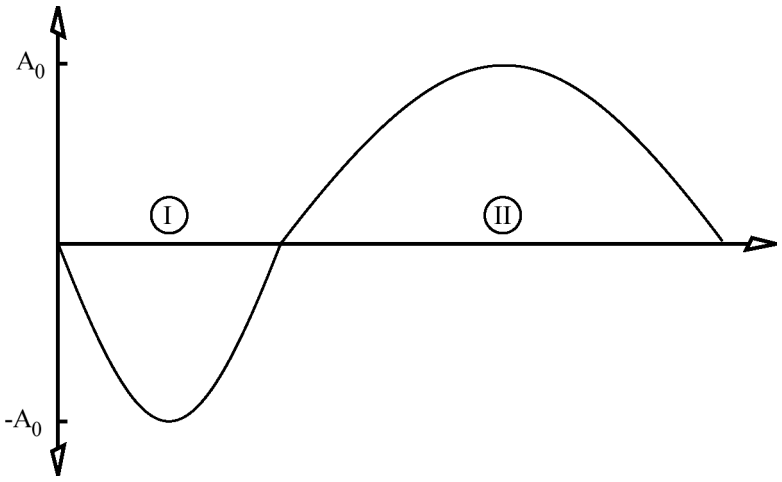



Figure 4.2. Piecewise Continuous Model of AM-FM Effects.

$$I)\ \Lambda_I(\omega_1 t) = -\sin(\omega_1 t) \qquad 0 \le \phi < \pi$$
$$II)\ \Lambda_{II}(\omega_2 t) = -\left(\frac{\omega_2}{\omega_1}\right)^2 \sin(\omega_2 t) \quad \pi \le \phi < 2\pi \tag{4.2}$$

And, thus, the DC value of the Amplitude ISF is:

$$\Lambda_{DC} = \frac{1}{\pi - 0}\int_0^{\pi} \Lambda_I(\omega_1 t) + \frac{1}{2\pi - \pi}\int_{\pi}^{2\pi} \Lambda_{II}(\omega_2 t) \tag{4.3}$$
$$= \frac{2}{\pi}\left[\frac{\omega_2 - \omega_1}{\omega_1^2}\right]$$

Now suppose there existed two complementary ideal rectifiers, one of which passed only the signal above the X-axis of Figure 2 ($v_P$), and the other only the signal below ($v_N$). The mean of the means of these rectifier outputs (i.e., the mean of the DC components of the rectified outputs) would then be of similar form as $\Gamma_{DC}$:

$$v_p(t) = \begin{Bmatrix} V(t) & for all\ V(t) \ge 0 \\ 0 & elsewhere \end{Bmatrix}$$
$$v_n(t) = \begin{Bmatrix} V(t) & for all\ V(t) \le 0 \\ 0 & elsewhere \end{Bmatrix} \tag{4.4}$$

$$\frac{\bar{v}_p(t) + \bar{v}_n(t)}{2} = \frac{A_0}{\pi}\left[\frac{\omega_1 - \omega_2}{\omega_1 \omega_2}\right]$$

As the effect of AM-FM is to slow down the half-periods of output waveforms Out and OutB similarly (i.e., Out $\neq$ -OutB) [24], an equivalent measure could be made by comparing the average of the maxima and minima of the output waveform to the common mode voltage available on the center tap of the tank inductor. This equivalent

measure is more amenable to circuit-level implementation: matched N- and PMOS peak detectors.

## 4.2 Proposed System / Implementation

Due to the increasing mixed-signal complexity of frequency synthesis subsystems, and of VCOs in particular, a modern frequency synthesizer contains multiple control loops, orthogonal in purpose (e.g., automatic level control, which maintains a constant oscillation amplitude of the VCO despite changing characteristic impedance over a wide tuning range [36]; or autonomous systems to select the appropriate frequency band in bandswitched VCOs [37],[38]) to the main phase locking intent of the PLL, and generally with very long time constants (as compared to the PLL).

This thesis proposes an autonomous system, which operates in conjunction with but independent of a PLL, which implements the $\Lambda_{DC}$ estimator of Section 4.1, and repetitively adjusts some aspect of a VCO core such that the point of minimal flicker noise upconversion is maintained despite perturbation away from this optima by PLL attempts to maintain phase lock. This thesis proposes a mixed-signal system which adjusts the relative size of P- to NMOS cross-coupled pairs in the oscillator core to this end, as shown in Figures 4.3–4.11. Mixed-signal adaption is proposed to avoid the inevitable phase noise impairment caused by analog adaption [36], in addition to the essential amenability of CMOS to digital implementations.

The complementary peak detectors of Section 4.1 are proposed to be implemented essentially as Meyer peak detectors [39], albeit in CMOS, and compared to each other, as opposed to a quiescent dummy (M25-26, M57-58 in Figure 4.4). As the N and P peak

detectors are compared to each other, it is essential that they match, which is essentially an Irish bull at radio frequencies: devices of unlike kind cannot have good relative matching over process, voltage, and/or temperature; and even trying to achieve some sort of matching at nominal process is a tradeoff between equivalating $g_m$ and $C_{gs}$. This thesis will attempt to match $g_m$ of the peak detectors by approximately scaling the width of the P peak detector in proportion to $\mu_P/\mu_N$, when biased at the same current as the N detector.

This inherently results in mismatch, and so some mechanism is needed to calibrate out this mismatch. This thesis proposes implementing the "mean of Peak N and Peak P" function as a *weighted* mean, where the weight is selected to cancel the mismatch or any other offsets that may exist in the circuit. This weighted mean function is proposed to be implemented by what is essentially a resistor-chain DAC (Figure 4.9), except that the N and P peak detector outputs are connected to VRef and VRefB, and the weight is selected by the digital word.

The mixed signal system in its entirety is shown in Figure 4.3, and is essentially a tracking ADC [40], clocked by CalClk, although it could also be implemented as a ramp or any other sort of low speed ADC. In fixed-frequency systems (that is, systems in which the frequency synthesizer is set to one frequency for a long time, as opposed to frequency hopping systems), CalClk could be an extremely low frequency (e.g., on the order of 1/(the required adaption time * $2^N$)), minimizing the power required for the subsystem.

The mixed-signal subsystem is comprised of an oscillator with integrated peak detectors (Figure 4.3), a weighted averager (Figure 4.9), an OTA-style continuous-time comparator (Figure 4.7), and a synchronous counter (Figures 4.6, 4.10, and 4.11) and

binary subtractor (Figure 4.5) of conventional CMOS design [41]. As a tracking ADC, the converter will start at whatever word was previously stored in the counter, and count one state up or down (the direction depending on the output of the comparator; which depends on the relative magnitudes of the weighted average of PkN and PkP versus the oscillators common mode voltage) for every active edge of CalClk. Upon reaching the desired state, the tracking converter will dither one LSB around the desired value (so-called 'bit bobble'). Upon cessation of CalClk, the last state will be stored in the counter and continue to be applied to the oscillator core.

As the VCO phase noise is degraded somewhat (even if only by the additional capacitive loading of the peak detectors) when the peak detectors are on, in practice the adaption loop should turned off after the appropriate P word has been found, for example after $2^N$ clocks for a tracking ADC. For all simulations below, the phase noise will be reported with the adaption loop off.

### 4.3 Initial Investigations: Varactor-less Oscillator

Initial investigations were performed with the simple oscillator of Figure 4.4, which has no varactor. The N- and PMOS effective widths are separately controlled by digital words N[4:0] and PB[4:0], respectively. Frequency tuning can be affected by changing the N and P words, but at the cost of also changing the bias point, as there is no current tail. The P word can also be tuned independently of N, but also at the cost of changing the bias point and frequency. This will necessitate the use of the FOM1

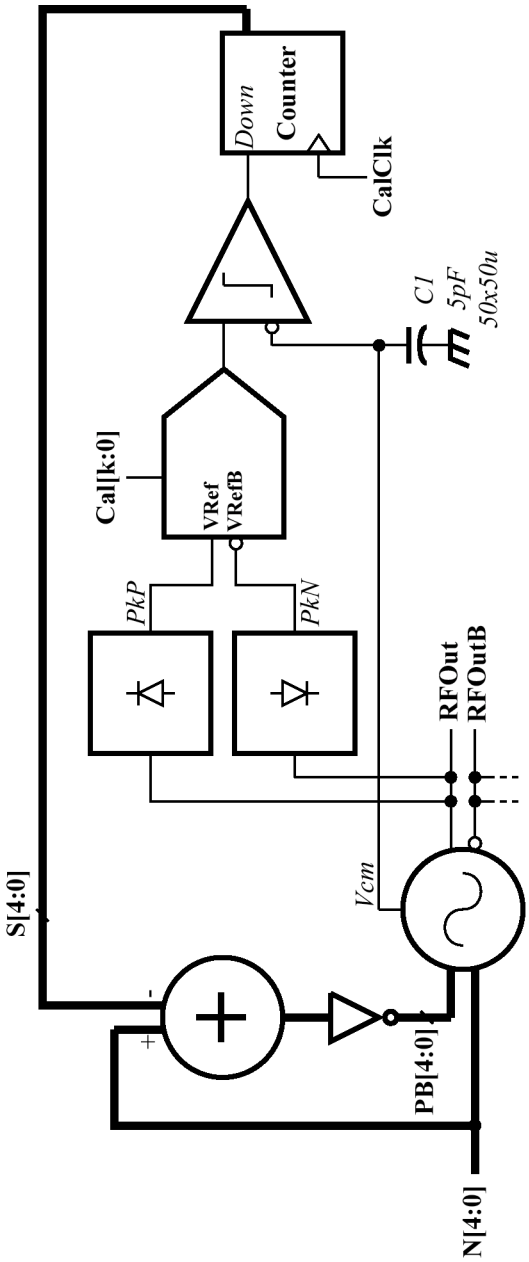



Figure 4.3. Top Level Schematic.

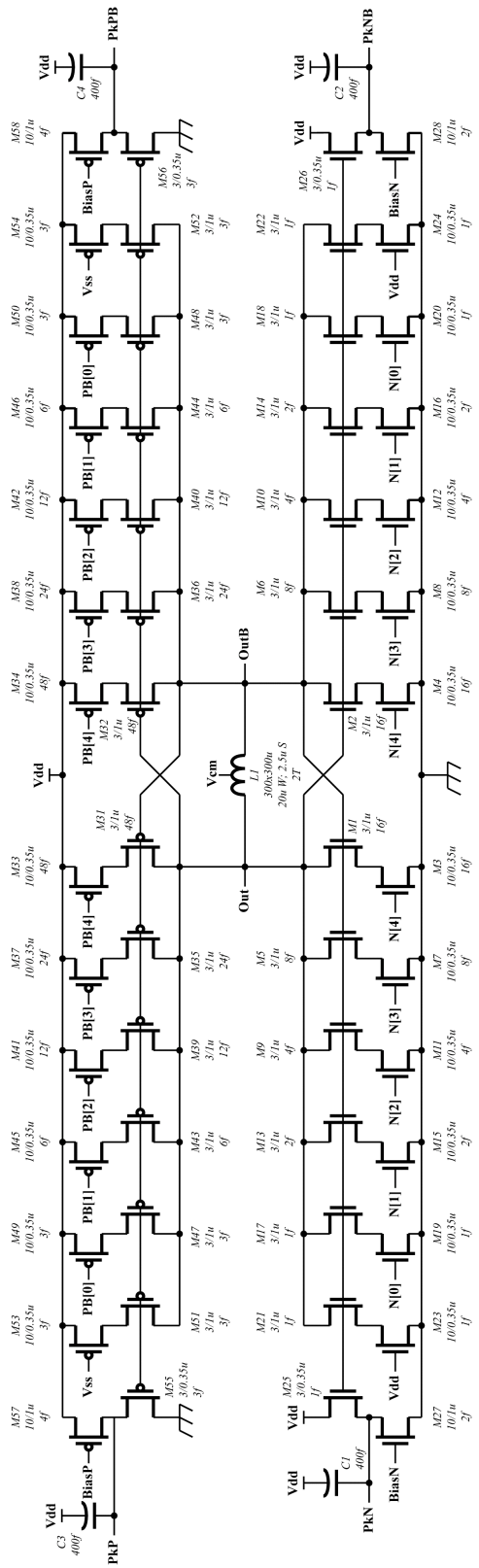



Figure 4.4. Oscillator Core used for Initial Investigations, with Integrated Peak Detectors.

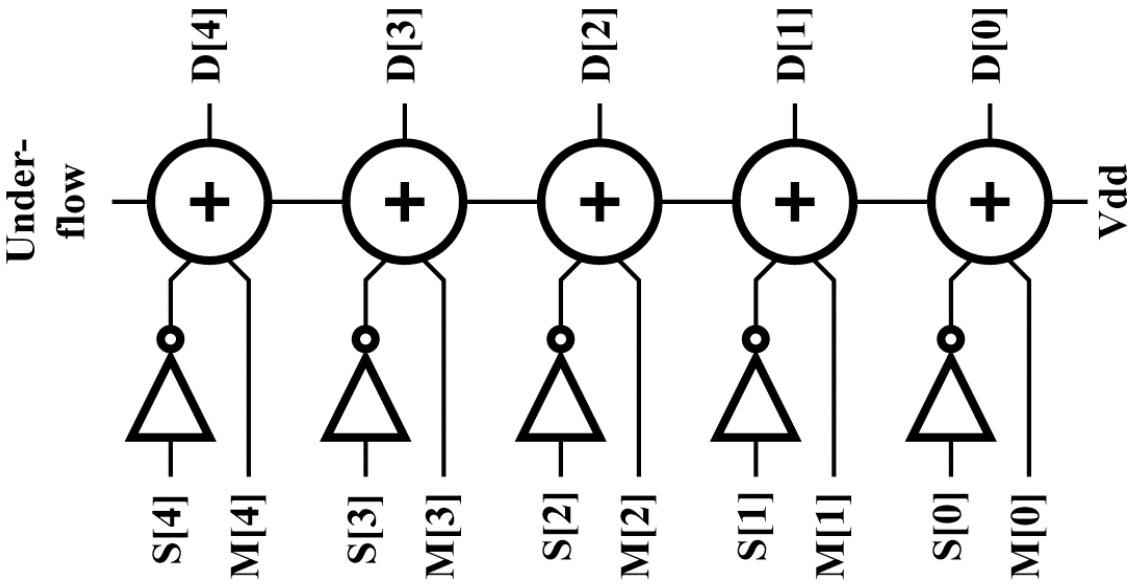



Figure 4.5. Five Bit Subtractor [41].

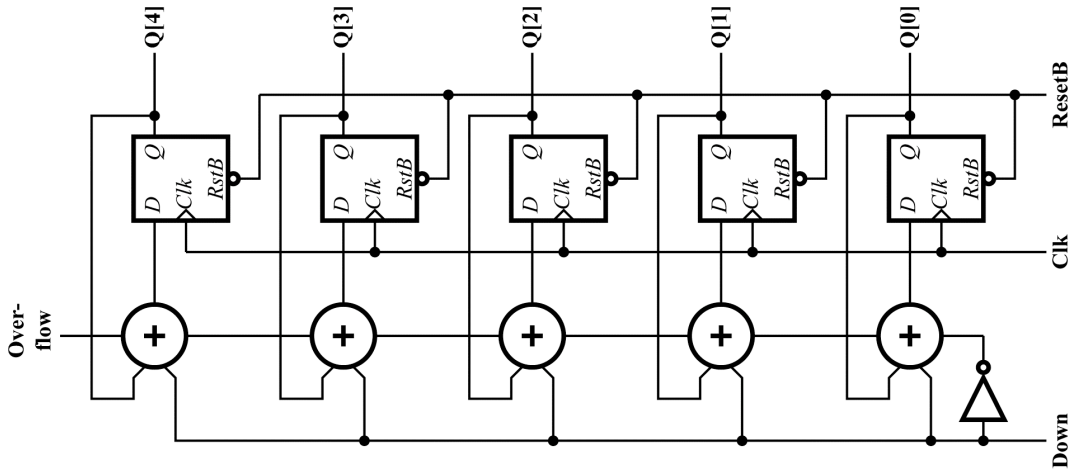



Figure 4.6. Five Bit Synchronous Up/Down Counter [41].

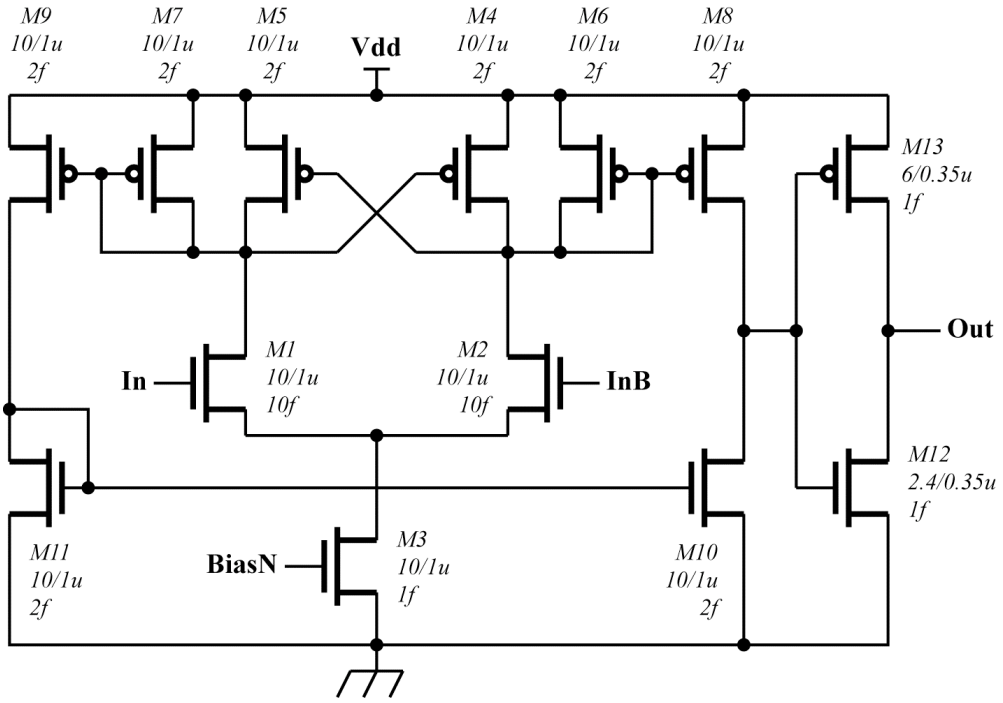



Figure 4.7. Continuous Time Comparator.

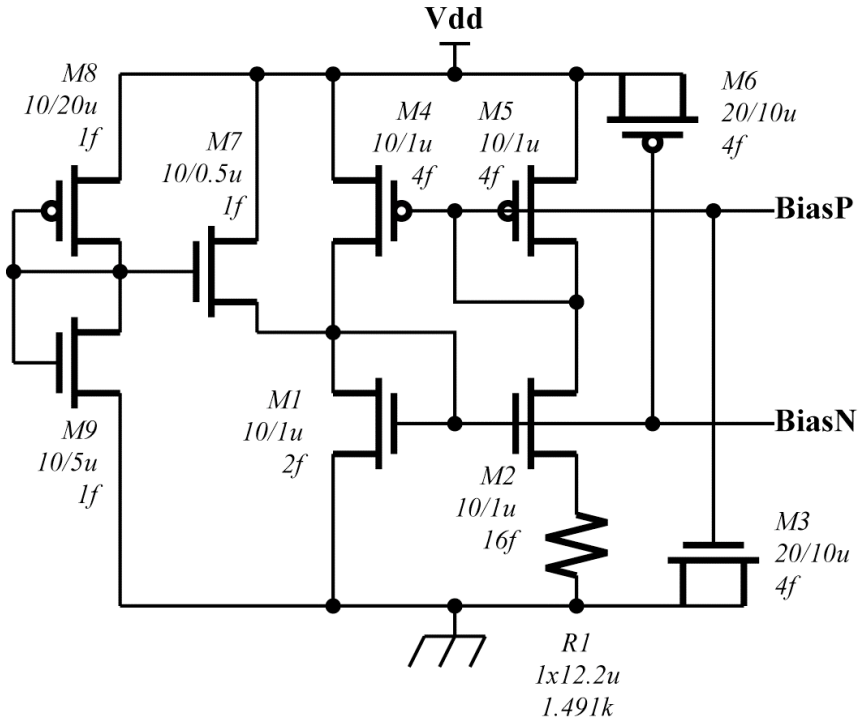



Figure 4.8. Simple PTAT Bias Source and Startup.

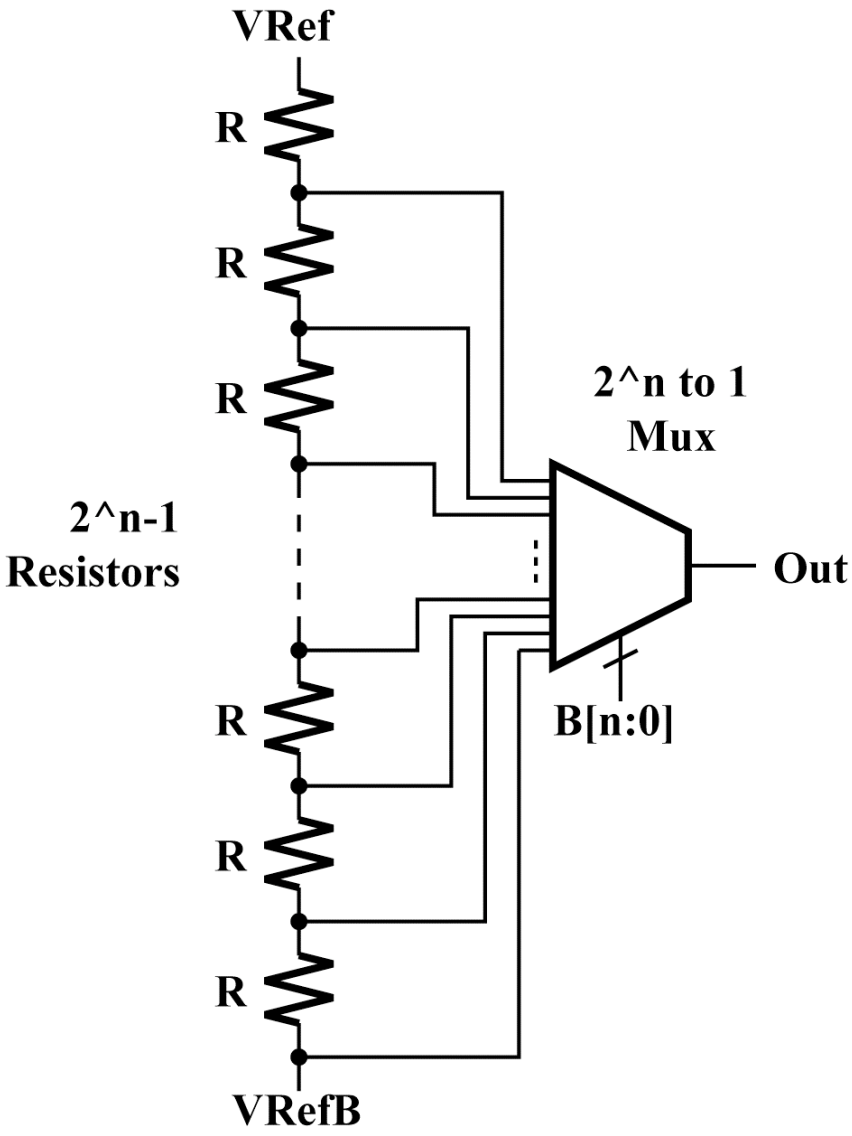



Figure 4.9. General Topology of Weighted Averager.

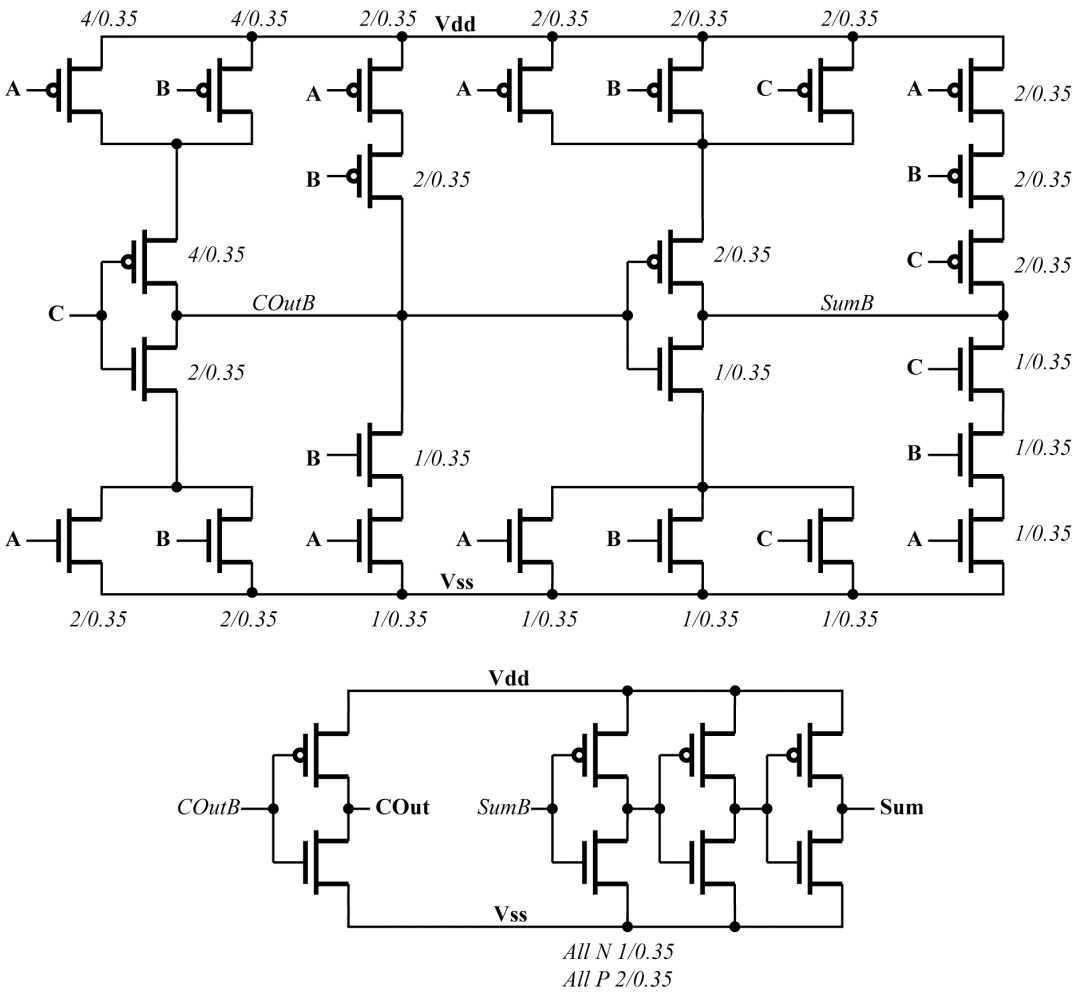



Figure 4.10. One Bit Adder.

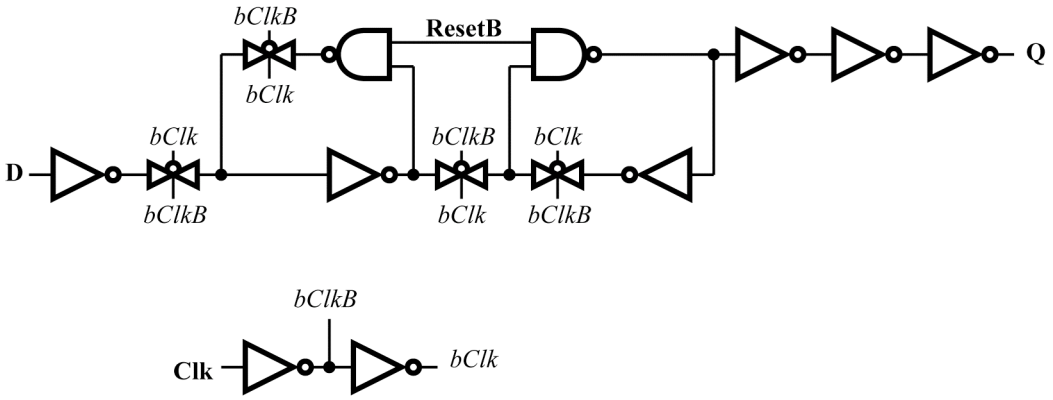



Figure 4.11. Register.

methodology of Section 2.4 to validate the effectiveness of relative tuning of the P word to minimize flicker noise upconversion. The appropriate calibration word (weight) needs to be determined, as well.

### 4.3.1 Simulation Methodology

Ideally, a transient simulation would be run with an arbitrary N word until bit bobble is observed, and then the P word would be recorded. After turning off the calibration subsystem, the FOM1 and FOM2 would be determined (via a frequency domain simulation, such as harmonic balance) for said N and P words. The estimator approach would be deemed a success if the reported P word produced the condition of minimum phase noise upconversion, for an arbitrary N word, using the same weight across all N.

Unfortunately, the above transient gedankensimulation would require an extremely long simulation time for the proposed system, due to the extremely large difference between the time constants of the oscillator (most likely gigahertz) and the calibration clock (possibly single digit hertz). An alternative simulation-by-parts approach is proposed: the calibration loop and oscillator/peak detectors are simulated separately. The calibration loop would be simulated with an ideal DAC replacing the oscillator/complementary peak detectors/weighted mean functionality, so as to validate the subsystem in a timely manner. The oscillator and peak detectors would be tested separately, with the entire P word space characterized, for both peak detector DC output voltages and phase noise, for selected N words. If the same weight causes the system to select the P word which minimizes FOM1 for all the selected N words, then the approach would be deemed a success.

One area of concern for such by-parts approaches is that something might be lost in the segmentation; such as the loading of the next stage. This is especially a problem for the peak detectors, which as circuits with low quiescent bias have minimal drive capability. Should loading prove to be an issue, buffering may be required.

### 4.3.2 Simulation Results: Oscillator and Peak Detectors

The simulations of the oscillator and peak detectors were performed on the testbench of Figure 4.12; the load resistance of 22kΩ was chosen to simulate the loading of the weighted averager. The simulation results are contained in Figures 4.13-4.19.

The resultant oscillation frequency, amplitude, and DC current versus state N = state P is shown in Figure 4.13. Note that both the oscillation frequency and amplitude change versus the state; thus the FOM1,2,3 methodology of section 2.4 will be needed to determine whether flicker noise upconversion varies versus state N or P.

A time domain plot of the oscillatory waveform and common mode and peak detector outputs is shown in Figure 4.14. Note the fundamental ripple on the peak detector outputs, as expected for half-wave rectifiers; and the second harmonic ripple on the common mode output. As the comparator bandwidth is much narrower than the frequency of oscillation, these ripple components do not affect the accuracy of the calibration loop.

The simulated FOM1, 2, and 3 versus P state for N[4:0]= 15 [01111] and N[4:0]= 31 [11111] are shown in Figures 4.15 and 4.16. Note the condition of minimum flicker noise upconversion (maximum FOM1) occurs at state 7 [00111] for N[4:0]= 15 and 22 for

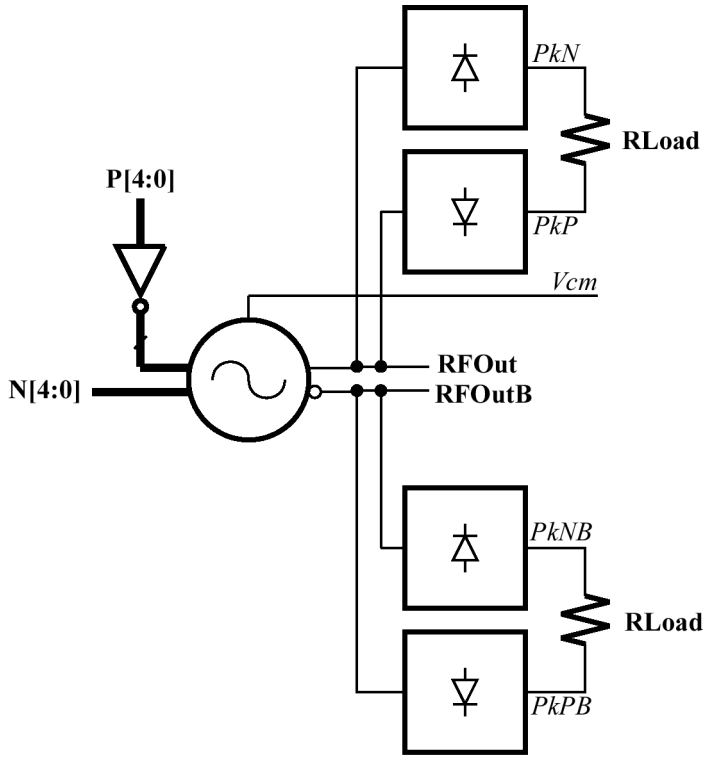



Figure 4.12. Simulation Testbench ($R_{LOAD}$ = 22 kΩ).

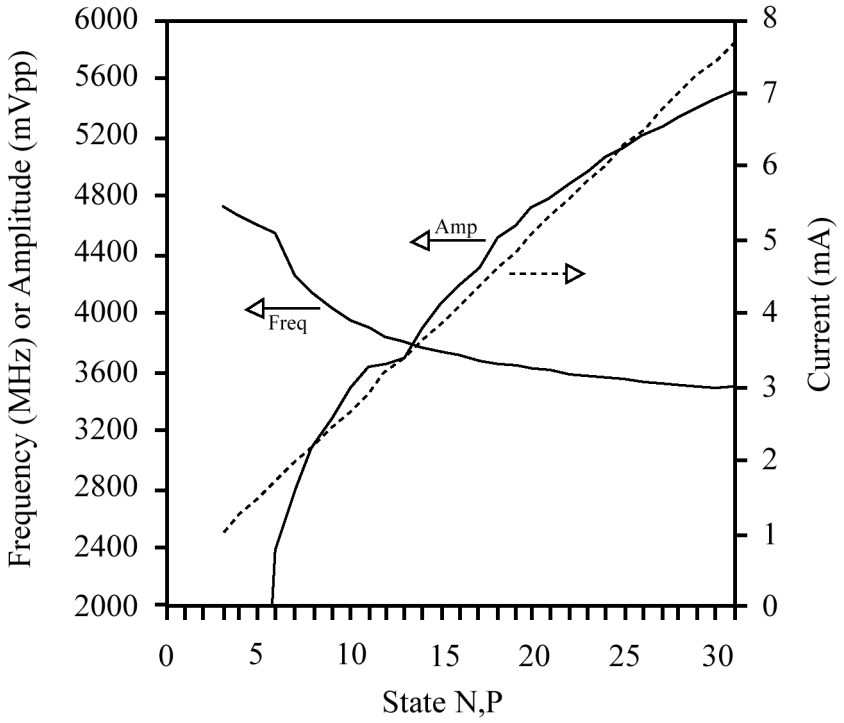



Figure 4.13. Simulated Oscillation Frequency, Amplitude, and Current Consumption Versus N,P State for the Oscillator of Figure 4.4.

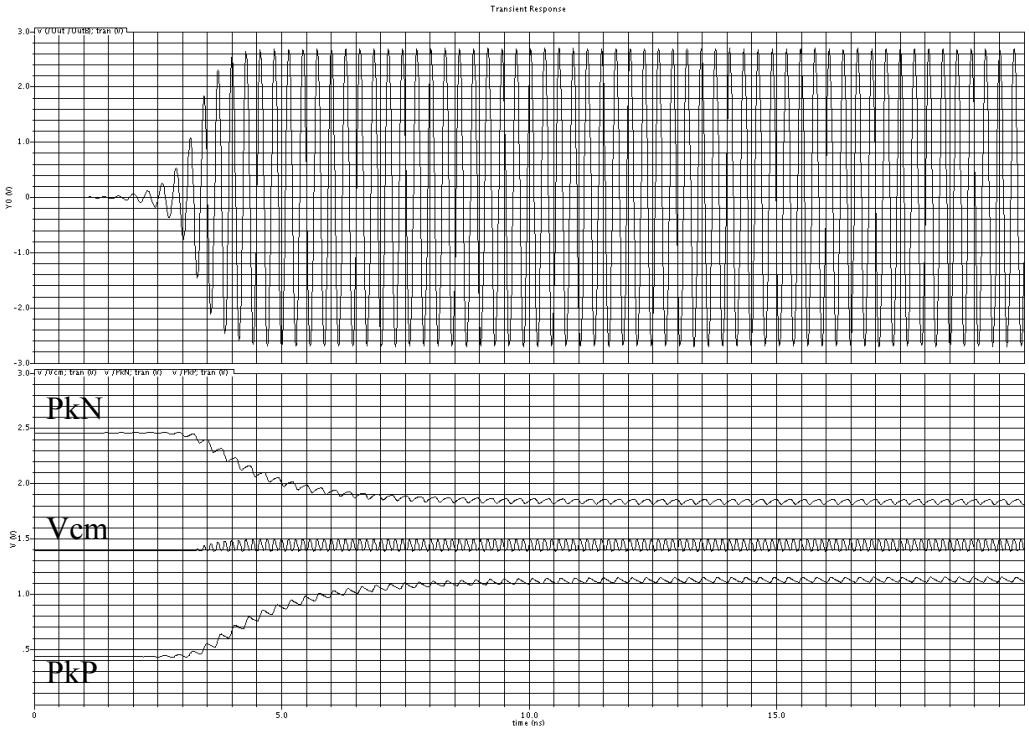



Figure 4.14. Simulated Output, Common Mode, N-Peak Detector, and P-Peak Detector Voltages Versus Time for the Oscillator of Figure 4.4 (N[4:0]=P[4:0]=[11111]).

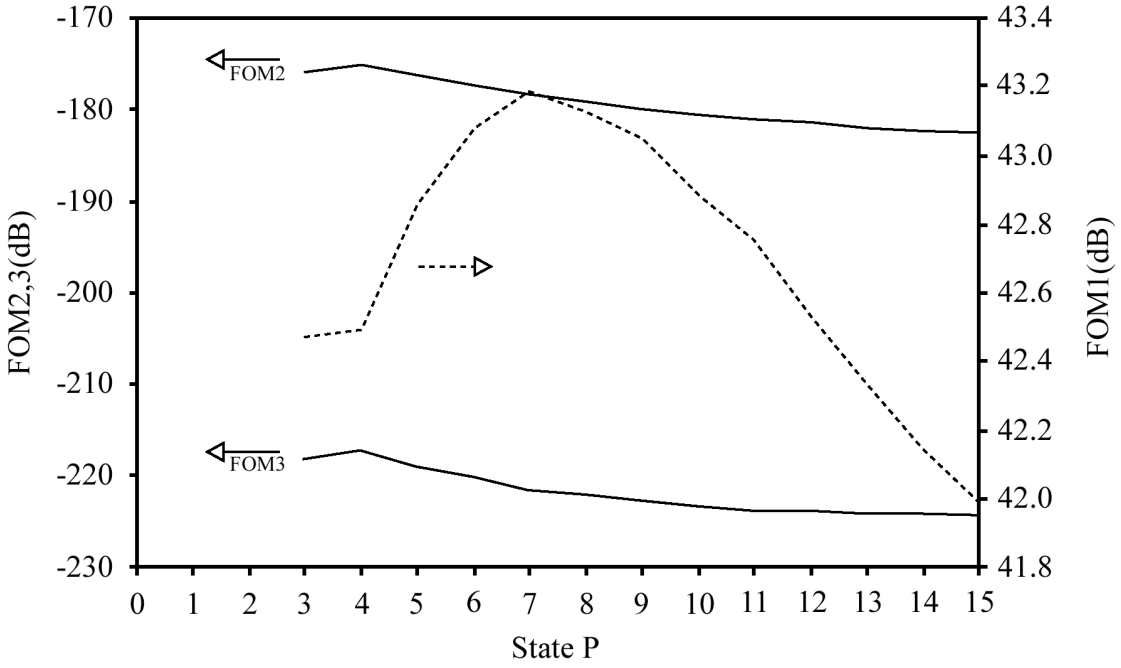



Figure 4.15. Simulated FOM1,2, and 3 for Oscillator of Figure 4.4, N[4:0]=[01111].

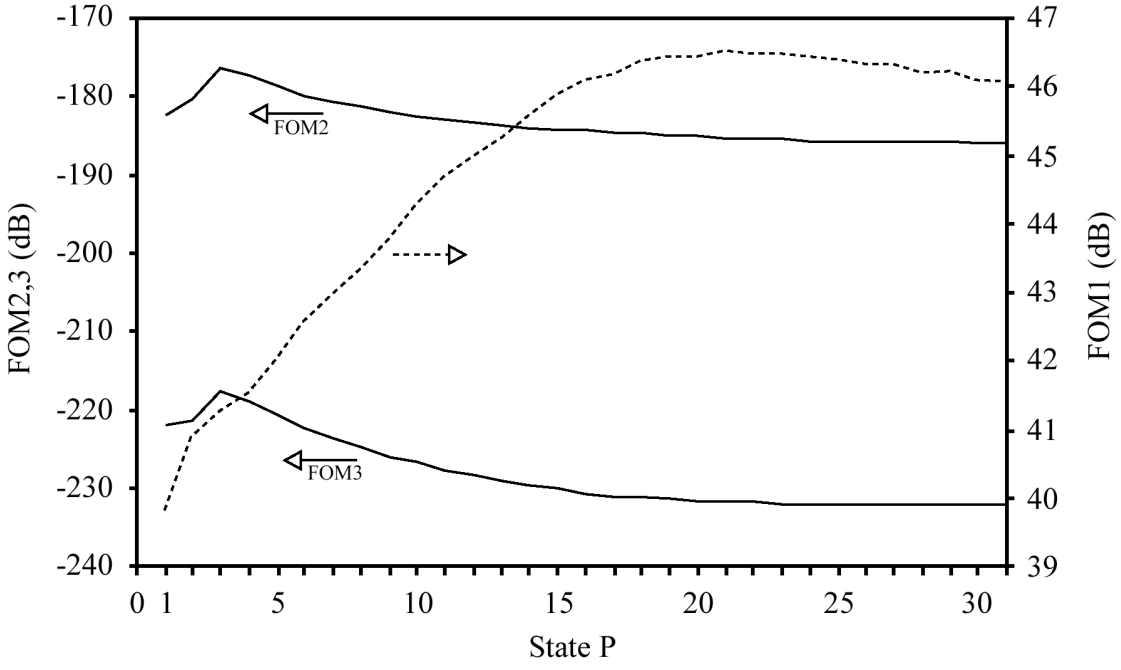



Figure 4.16. Simulated FOM1,2, and 3 for Oscillator of Figure 4.4, N[4:0]=[11111].

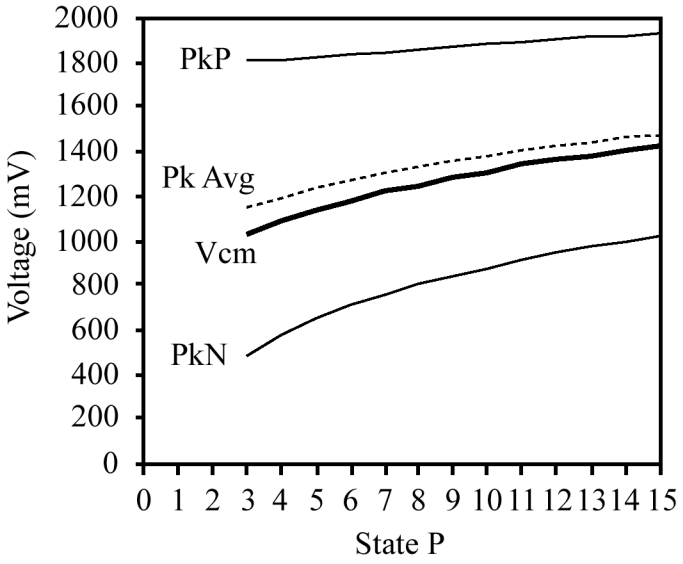



Figure 4.17. Simulated Common Mode and Peak Detector Voltages for Oscillator of Figure 4.4, N[4:0]=[01111].

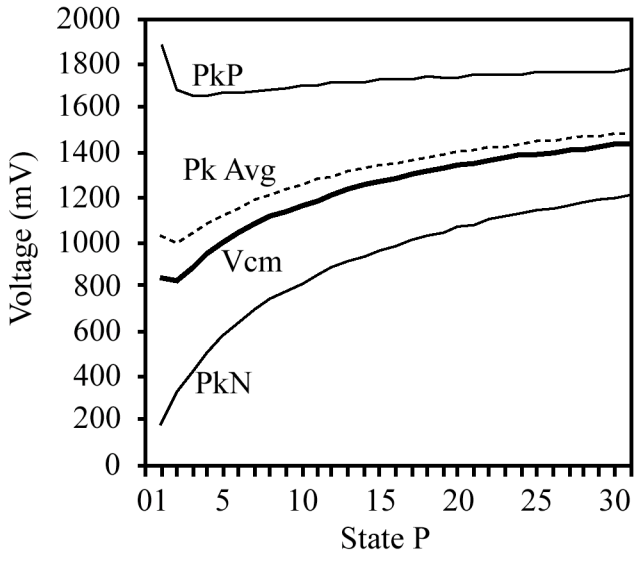



Figure 4.18. Simulated Common Mode and Peak Detector Voltages for Oscillator of Figure 4.4, N[4:0]=[11111].

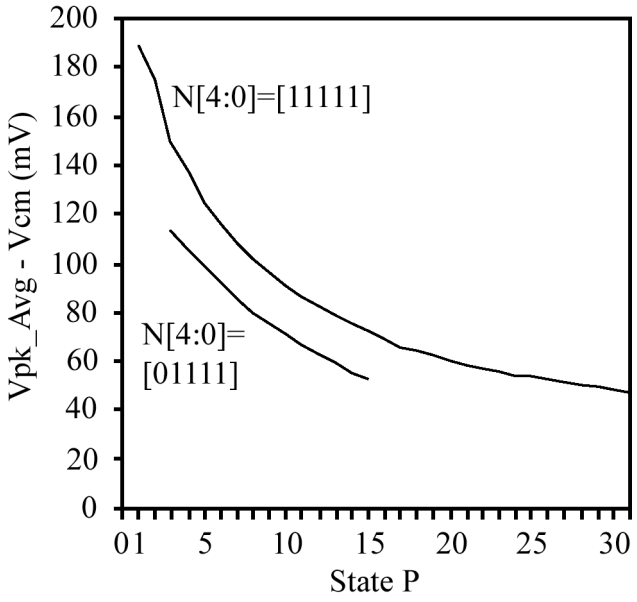



Figure 4.19. Simulated Difference Between the Average of the Peak Detectors and the Common Mode Voltage for Oscillator of Figure 4.4.

N[4:0]=31. Given the minimal sources of AM-FM in this circuit (i.e., if the peak-to-peak single-ended swing is constrained to be less than $V_{DD} - V_{GS,N} - V_{GS,P}$, then the tank capacitance is to the first order constant; if the swing is greater, but $g_{m,N} = g_{m,P}$ and $C_{GS,N} = C_{GS,P}$, then the waveform distortion would be single-ended symmetric, and thus not increase $\Lambda_{DC}$.), it is reasonable to expect the condition of minimum flicker noise upconversion to be the compromise between equivalent N and P $g_m$ and $C_{GS}$ which maximizes 'push' and 'pull' single-ended symmetry.

For N[4:0]=31, assuming the switches to be ideal, the P[4:0] word which produces an equivalent $G_m$ is 28.9; Equivalent $C_{GS}$ is 9.7. For N[4:0]=15, the P[4:0] word which produces an equivalent $G_m$ is 13.9; equivalent $C_{GS}$ is 4.3.

The peak detector output and common mode voltages are shown in Figure 4.17 (N[4:0]=15) and Figure 4.18 (N[4:0]=31); and summarized in Figure 4.19. The difference between the average of the peak detector voltages and the common mode voltage which corresponds to the state of minimum flicker noise upconversion is 85.3mV for N[4:0]=15 and 57mV for N[4:0]=31. Using the mean of these two values (71.2mV) for both N[4:0] cases would result in a FOM1 degradation of less than 0.7dB in either case.

### 4.3.3 Final Weighted Mean Circuit

Using the simulated common mode and peak detector voltages developed in Section 4.3.2, the final weighted mean circuit can be built: Figure 4.20. A resolution of five bits in conjunction with large terminator resistors on the ends of the resistor divider allows for a resolution of 5 mV and range of 155 mV for the N[4:0]=31, P[4:0]=22 case. The optimum calibration word (i.e., the calibration word which made the peak detector weight

average as nearly equal to the common mode voltage as the DAC resolution allowed, for the P State which produces minimal flicker noise upconversion) was found to be 7 for the N[4:0]=31 case, and 8 for the N[4:0]=15 case. A compromise value of Cal[4:0]=7 was used for the net system simulation, below in Section 4.3.5.

### 4.3.4 Simulation Results: Calibration Subsystem in Isolation

Using the weighted averager of Section 4.3.4, the greater portion of the calibration subsystem was next tested in isolation. The testbench is shown in Figure 4.21. Simple logic blocks such as the subtractor were not included, as they were considered of low risk to failure, and as the omission speeded up the simulation significantly.

The simulated results are shown in Figure 4.22. The upper chart in the figure shows the calibration clock; the lower chart shows the reference input into the comparator and the output of the DAC (the weighted averager). Note that the system increases the output of the DAC until it exceeds the reference voltage, and then the output dithers around the reference voltage (bit bobble). Also note that the output value is preserved even after the calibration clock terminates.

### 4.3.5 Simulation Results: Net System Simulation

With the confidence that arose from successful simulations-by-parts, the net system of Figure 4.3 was finally simulated, using a compromise calibration word of Cal[4:0]=7. A calibration clock frequency of 10 MHz was used. The simulation results are shown in Figure 4.23.

For the entire simulation period, N[3:0] = [1111]. Initially, N[4]=0, but at 3.2uS, N[4] is changed from 0 to 1. This is shown in the middle trace of the figure, along with the calibration clock. Thus, the convergence of the system for N[4:0]=15 is shown during the first half of the simulation, followed by N[4:0]=31. The upper trace shows the P[4:0] word, as converted through an ideal DAC of gain 1V/bit, and the bottom trace shows the output of the weighted mean circuit (dashed line) and the common mode voltage (solid line).

Note that the P State dithers between 7 and 8 for N[4:0]=15, and 20 and 21 for N[4:0]=31, nearly the +/- 0.5*LSB ultimate resolution achievable by a tracking ADC. This represents a degradation of FOM1 of 0.1 dB, worst case, as compared to the best achievable error of a tracking ADC (+/-0.5*LSB) of 0.1 dB.

### 4.4 Further Investigations: Voltage Controlled Oscillator

It was expected that an oscillator with more pronounced AM-FM (i.e., a voltage-controlled oscillator with a strong varactor) would more strongly show the advantages of the approach. To that end, the voltage controlled oscillator of Figure 4.24 was designed and simulated: the N-width is as N[4:0]=31 for the circuit of Figure 4.4. The P-width programmability is also equivalent to Figure 4.4. A current tail is included (to more isolate the bias point from the programmed width), as is a MOS varactor DC-coupled to the mid-rail nodes.

The FOM1,2, and 3 are shown for an oscillation frequency of 4.7GHz (Figure 4.25) and 4.8GHz (Figure 4.26). In both cases, the varactor voltage was adjusted per P State to

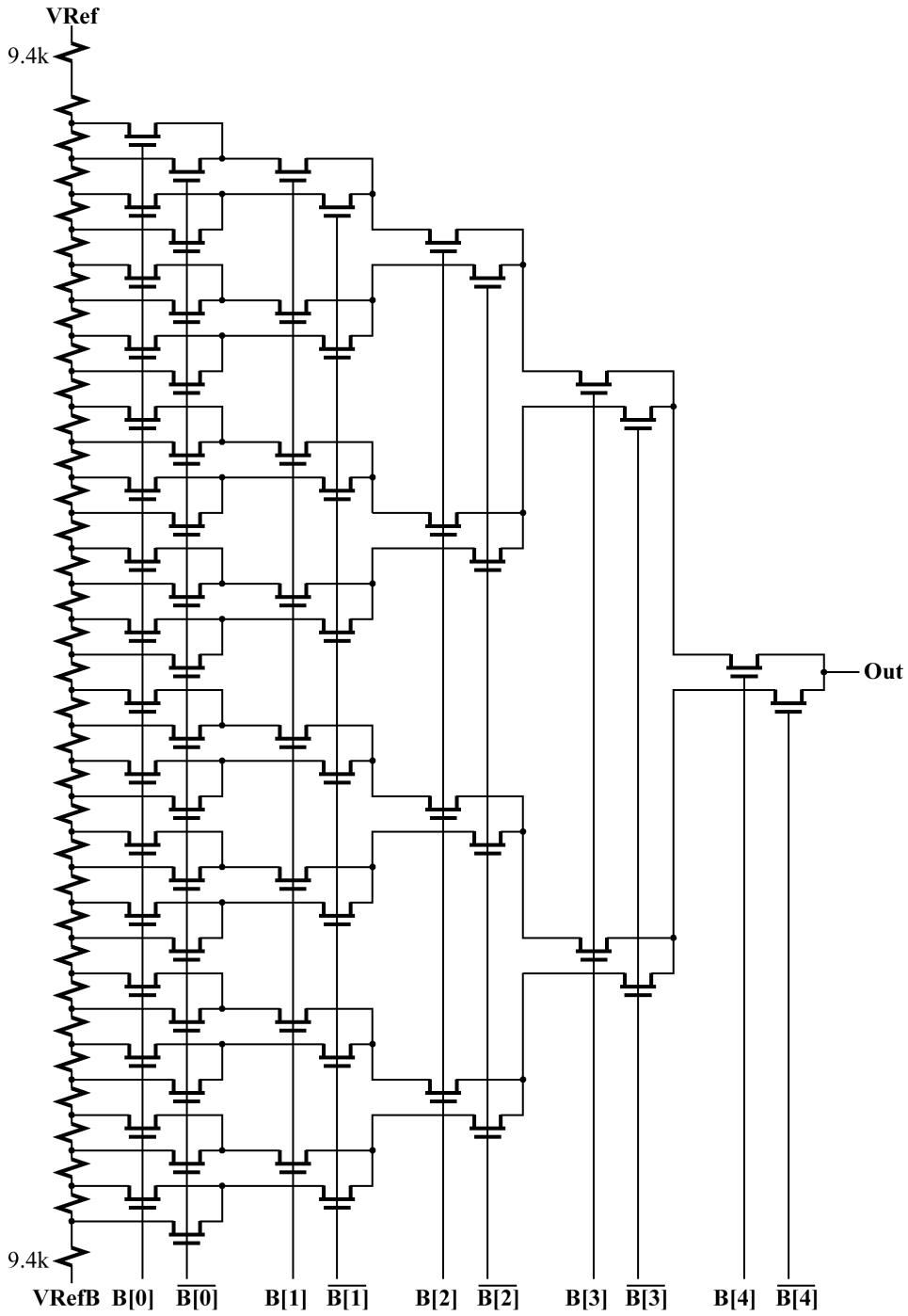



Figure 4.20. Final Weighted Mean Circuit (All resistors 204.7Ω unless specified, all MOSFETs 10/0.35 μm).

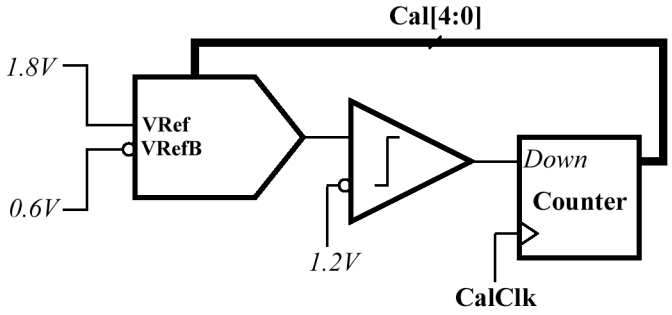



Figure 4.21. Calibration Loop Testbench (Weighted Mean circuit of Fig. 4.20).

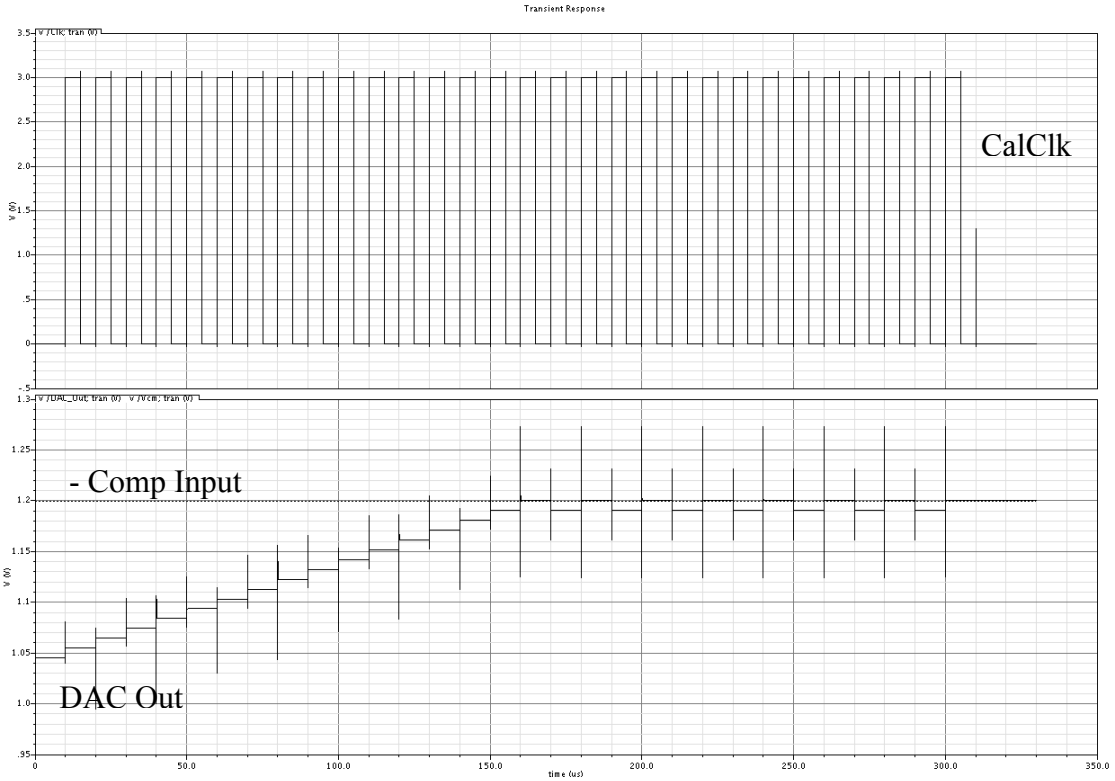



Figure 4.22. Simulated Calibration Loop without Oscillator (Testbench of Fig. 4.21).

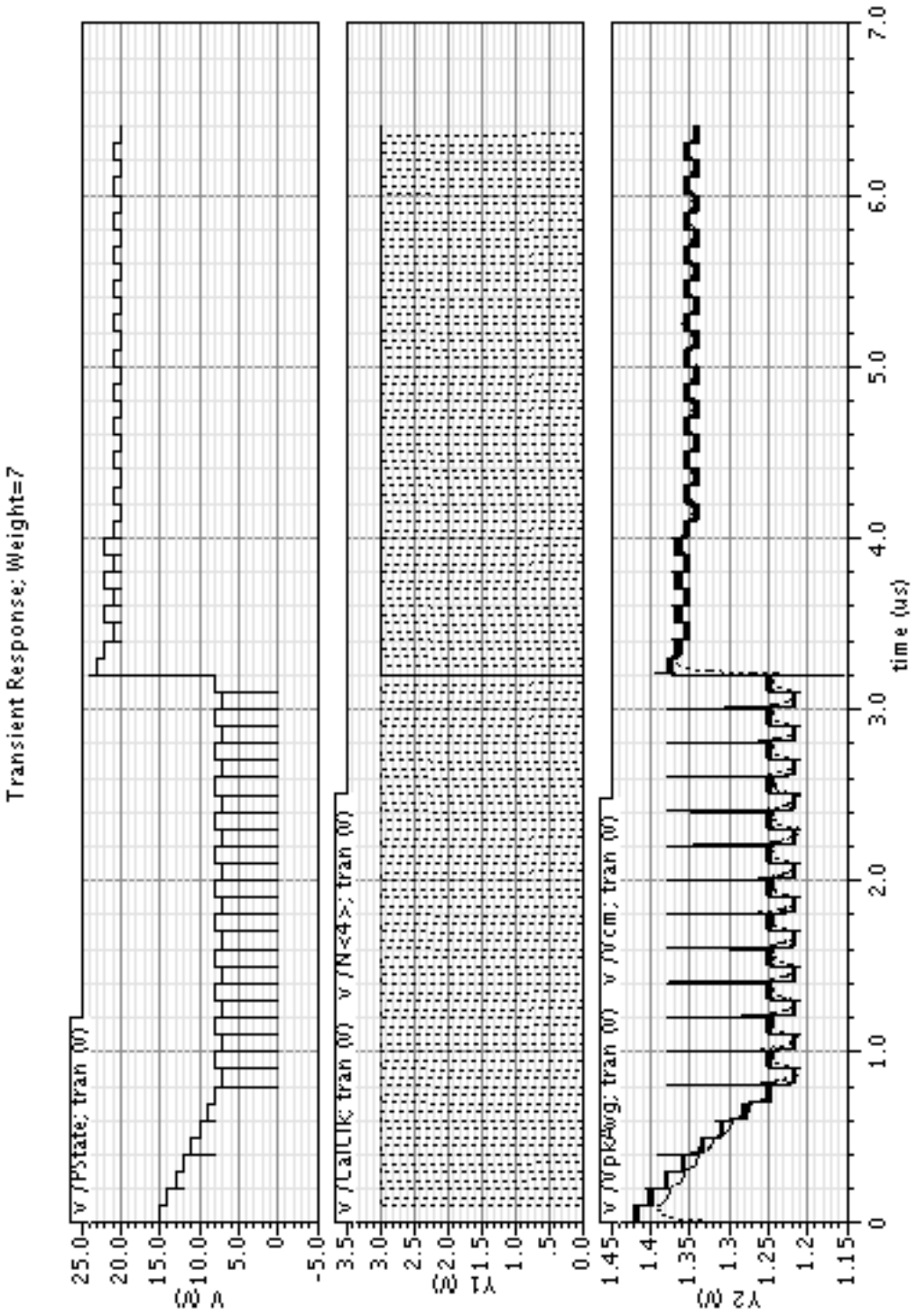



Figure 4.23. Net System Simulation (Testbench of Fig. 4.3; Weight=7).

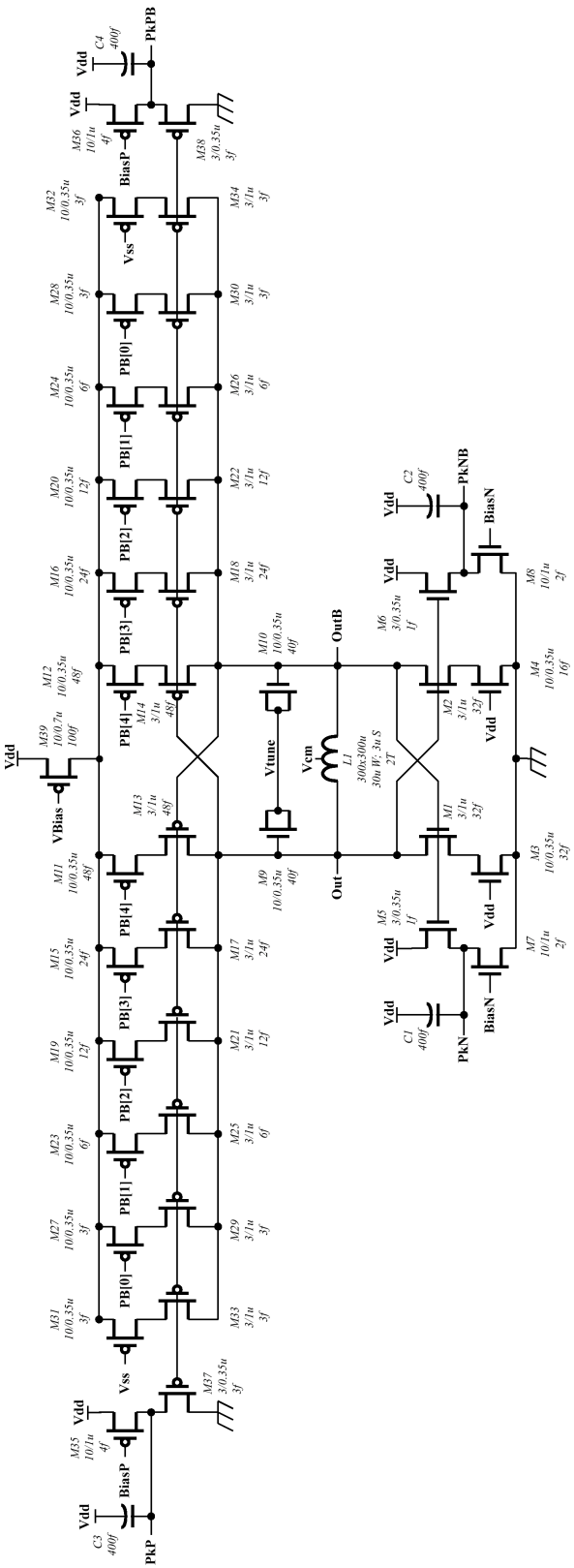



Figure 4.24. Voltage Controlled Oscillator (PBulk = Vdd for Osc devices; Source for Switches).

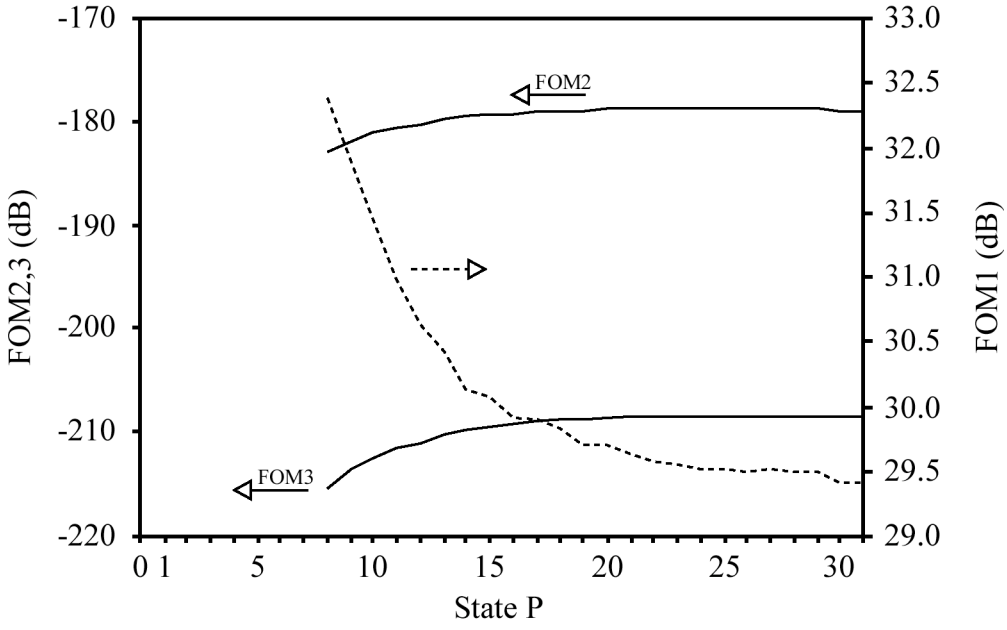



Figure 4.25. Simulated FOM1,2, and 3 for Oscillator of Figure 4.24, $f_{OSC}$=4.7GHz.

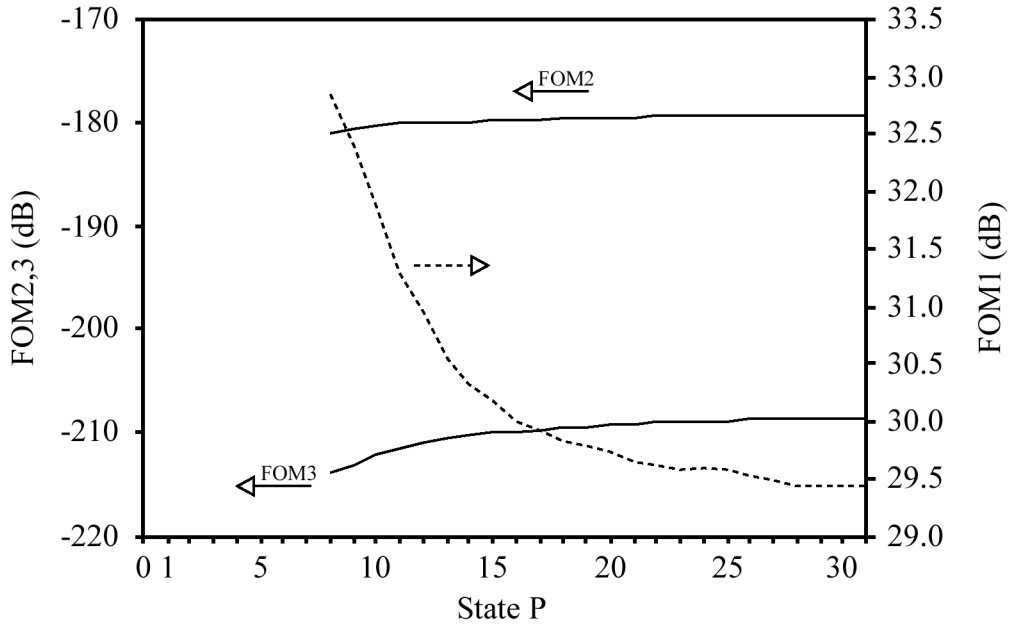



Figure 4.26. Simulated FOM1,2, and 3 for Oscillator of Figure 4.24, $f_{OSC}$=4.8GHz.

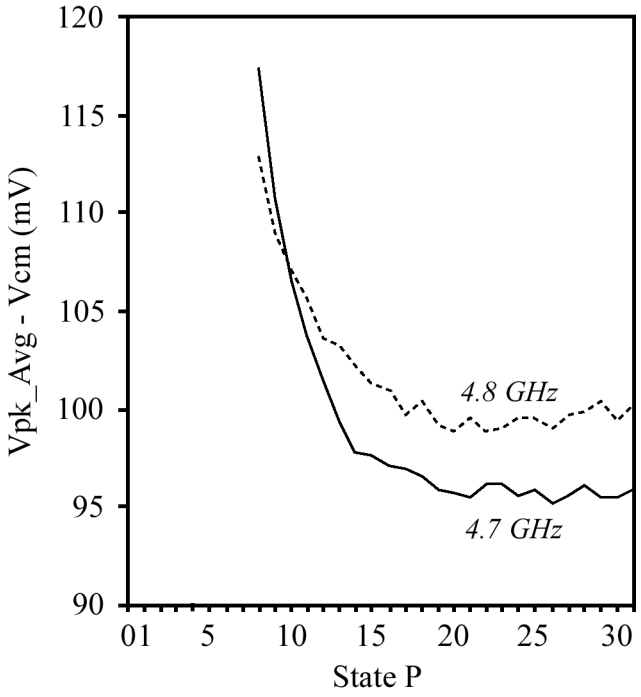



Figure 4.27. Simulated Difference Between the Average of the Peak Detectors and the Common Mode Voltage for Oscillator of Figure 4.24, fosc=4.7 and 4.8 GHz.

maintain a constant frequency of oscillation, simulating in a DC sense a PLL operating in conjunction with the calibration subsystem. Note that maximum FOM1 occurs for P state 8 in both cases: the oscillator would not start up for P states smaller than 8.

It is not surprising that the P-State which minimizes flicker noise upconversion should be smaller than the P-State for the circuit of Figure 4.4 with equivalent N-width (that is, the FOM1 of Figure 4.16), for there significantly greater sources of AM-FM in this circuit as compared to that one. In particular, the varactor capacitance will increase as the mid node instantaneous voltage increases, slowing down the "tops" of the single-ended oscillatory waveforms as compared to the "bottoms." This, in turn, would require less P "pull" than N "push" to try to equalize the "top" and "bottom" areas of the waveform.

The peak detector average and common mode voltages are shown in Figure 4.19. The difference between the average of the peak detector voltages and the common mode voltage which corresponds to the P state of minimum flicker noise upconversion (state 8) is 117.4mV for 4.7 GHz; 112.9 mV for 4.8 GHz. Using the average of these two values (115.1 mV) would represent a state of error for either case.

# CHAPTER V

# CONCLUSIONS

The mechanism by which flicker noise in the active devices in oscillatory cores upconverts to sidebands around the oscillation frequency, originally described as the result of "nonlinearities" by Leeson [14], and later with less concision by Hajimiri [16], Hegazi [15], and others is at the crux of any exercise to minimize $1/f^3$ noise in oscillators. Essentially, the exercise can be broken into two nearly orthogonal tasks: minimizing flicker noise generation, and minimizing flicker noise upconversion.

The first task, although in practice perhaps not simpler to achieve, is conceptually simpler to comprehend. Minimizing flicker noise generation can be done by improving device physics, increasing device size, and/or eliminating unessential components which contribute noise. The ubiquitous cross-coupled negative resistance oscillator is usually implemented with a current tail, the elimination of which is shown [29] to substantially improve $1/f^3$ noise, but at the cost of reduced common-mode rejection and sensitivity of the bias point to PVT. The core devices, as well, can be sized to reduce flicker noise, to some extent.

The second task, as detailed by Hajimiri and Hegazi, is somewhat subtler. The two approaches, although perhaps equivalent in their ends, are quite different in their means. The Hegazi [15] approach is essentially a Fourier decomposition exercise, describing by analogy to frequency mixing the upconversion pathways of flicker noise. As such, it is primarily interested in the frequency translation of very small signals (noise). The primary take-away is that signals at harmonics and sub-harmonics of the oscillation frequency should be filtered as well as possible.

The Hajimiri approach [16], on the other hand, quantifies the flicker noise upconversion gain in terms of properties of the single-ended time domain oscillatory waveform. The $1/f^3$ corner is proportional to the device flicker corner and $(\Gamma_{DC}/\Gamma_{RMS})^2$, where $\Gamma$ is, in general, complicated to calculate, but approximately the derivative of a sinusoidal waveform. Insofar as AM-PM is a dominant contributor to the noise, $\Lambda_{DC}$ may be an indicator of noise in the $1/f^3$ region, as well. If a waveform may be approximated as a piecewise composition of half-sinusoidal segments, as argued in chapter four for the waveforms present in CMOS LC oscillators, then the asymmetry of the waveform itself may be used as an estimator of $\Lambda_{DC}$.

This estimate is, of course, only useful in cases were the waveform asymmetry may be reasonably modeled by piecewise half-sinusoids. Ring oscillators, with their nearly square-wave oscillatory waveforms and potentially unequal rise- and falltimes, for example, are a case where it is clearly not applicable. Cross-coupled negative-resistance CMOS LC oscillators, with their inherent harmonic filtering and waveform asymmetry dominated by signal-dependent capacitances, on the other hand, do seem to be reasonably represented.

The simple estimator thus developed was shown to be useful in estimation and adaptive control of $\Lambda_{DC}$ in the varactor-less CMOS LC oscillator of section 4.3. The adaptive control was implemented by a circuit which is essentially a tracking ADC, where the weighted mean of the complementary peak detectors is compared to the common-mode voltage, and the oscillator P-width is adjusted to the point of minimum flicker noise upconversion. Although slightly different offset voltages (the offset between the mean of the peak detector voltages and the common mode voltages), which is

presumed to be dominated by mismatch between the N- and PMOS peak detectors, were shown to produce the condition of minimal flicker noise upconversion in the N[4:0]=15 and N[4:0]=31 cases, the difference was small. Using the mean of the two voltages for both cases resulted in less than 0.7dB degradation of FOM1 from the peak FOM1.

Further investigation with a VCO showed continued validity of the approach, and suggested that very wide-tuning VCOs with "strong" varactors might benefit from the approach, assuming the condition of optimum $FOM_1$ might be found for each frequency of oscillation.

As shown above, the $FOM_1$, $_2$, and $_3$ methodology developed in section 2.4 proved to be very useful in identifying the relative amount of flicker noise upconversion, despite varying bias points, and thus varying $FOM_2$. Although extensive benchmarking of $FOM_1$ to flicker noise performance was not done, it is interesting to note that the circuit of Figure 4.4, with minimal sources of AM-FM, has about 14dB better $FOM_1$ than that of Figure 4.24. It is hoped that future work will adopt the $FOM_{1,2}$, and $_3$ methodology, so that the best-in-class $FOM_1$ may be known.

## 5.1 Unique Contributions

The unique contributions of this research lie in three separate areas, namely (1) the simple $\Lambda_{DC}$ estimator, and method of application; (2) the $FOM_1$ methodology to assess the effectiveness of (1); and (3) a proposal as to how to apply the cycling-to-accumulation technique to continuous time oscillators. These contributions are summarized in Table 5.1.

Table 5.1. Unique Contributions of this Research.

| *Category* | *Contribution* |
|---|---|
| $\Lambda_{DC}$ Estimator | Simple $\Lambda_{DC}$ hardware estimator for CMOS LC Oscillators which are AM-FM dominated in the $1/f^3$ region. |
| | Adaptive oscillator and method of adaption (which is similar to a tracking ADC), which repeatedly adjusts the oscillator to maintain the condition of minimum flicker noise upconversion, based on the $\Lambda_{DC}$ estimate. |
| $FOM_1$ Methodology | Figure Of Merit proportional to total upconverted flicker noise, independent of 20 dB/decade region performance. |
| Cycling-to-Accumulation for Continuous Time Oscillators | An approach is proposed which would allow the cycling-to-accumulation strategy for minimizing flicker noise generation be applied to continuous time oscillators, but is not rigorously vetted. |

One conference publication, which is essentially an abridgement of chapter four, has resulted from this research:

D.S. Douglas and J.S. Kenney, "Estimation and Adaptive Control of the DC Component of Impulse Sensitivity Functions in CMOS LC Oscillators," *IEEE Radio and Wireless Symposium*, Orlando, January 22-24, 2008, P1-46.

## 5.2 Significance of Contributions

The $\Lambda_{DC}$ estimator and its method of application represent the first published hardware estimator for an Impulse Sensitivity Function quantity, albeit for the special case of CMOS LC oscillators. As such, this work extends the Hajimiri Impulse Sensitivity Function theory from a purely analytical approach to something which may be physically quantified by in-circuit test measures and adaptively minimized. However, this research does not easily generalize to all ISF quantities or all oscillators.

## 5.3 Future Work

It is hoped that future work will develop generalized estimators for Impulse Sensitivity Function quantities. Generalized in this case means both general in type of quantity estimated (i.e., $\Lambda_{DC}$, $\Lambda_{RMS}$, $\Gamma_{DC}$, and $\Gamma_{RMS}$) and in type of oscillator to which the estimator may be applied (i.e., LC, Ring, etc.). A generalized estimator will be required to operate on a multitude of oscillatory waveforms, and thus a synergistic similarity between the Impulse Sensitivity Function quantity desired and the oscillatory waveform cannot generally be assumed. Therefore, a simple single analog signal processing component (the peak detectors, in this case) is not, in general, sufficient. However, perhaps a small number of configurable analog signal processing components will be versatile enough to span a large portion of the "ISF quantity-oscillator type" space.

The promise of the cycling-to-accumulation approach is tempered by current simulation tools' limited capability with non-stationary noise sources. As such, it seems both a promising (straight-forward approach, appropriate scope) and non-promising (tapeout required) topic for a Master's thesis.

# APPENDIX A

## DEVELOPMENT OF THE $\Gamma_{DC}$, $\Lambda_{DC}$ FOR THE WAVEFORM OF FIGURE 4.2

Four different methods of computing the ISF are presented in [16],[17]; some exact and some approximate. Although the "ISF of an Ideal LC Oscillator" approach of [17] will be used below, all of the exact methods produce the same answers for the ISFs. Essential for computing the ISFs is some assumption as the cause of the "instantaneous frequency" change at the transition from region I to region II: step capacitance change or step inductance change? In light of the actual physical mechanisms of interest, step capacitance change will be assumed.

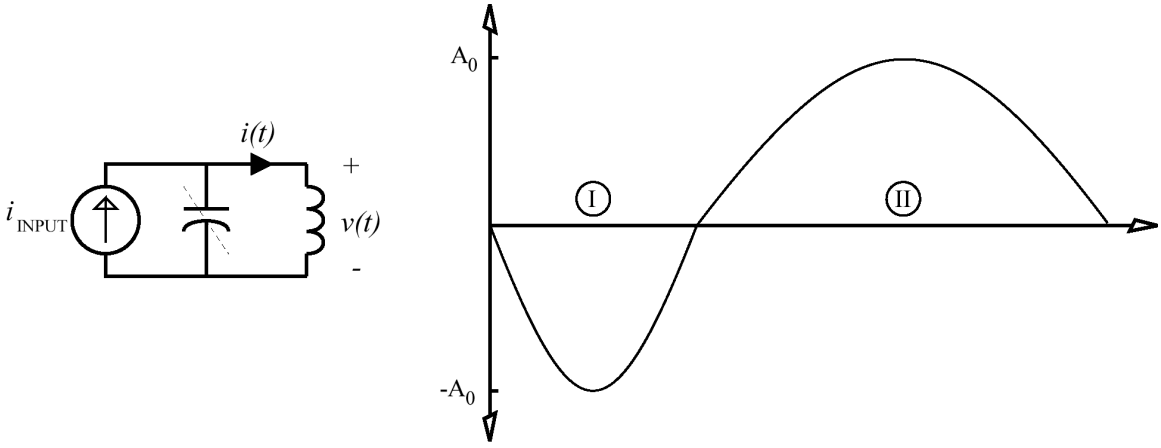



Figure A.1. Ideal Piecewise Continuous Oscillator and Waveform.

Assuming a step capacitor change at the transition from (I) to (II):

$$\begin{aligned}
&\omega_1 \geq \omega_2 \\
&\omega_1 = \frac{1}{\sqrt{LC_1}} \\
&\omega_2 = \frac{1}{\sqrt{LC_2}} \\
&L = \frac{1}{\omega_1^2 C_1} = \frac{1}{\omega_2^2 C_2} \\
&C_2 = C_1\left(\frac{\omega_1}{\omega_2}\right)^2
\end{aligned} \tag{A.1}$$

Letting $C_1$=C, then

$$C_2 = C\left(\frac{\omega_1}{\omega_2}\right)^2 \tag{A.2}$$

The output voltage and current through the inductor at time *t* are:

$$\begin{aligned}
&(I)\ \ v(t) = -A_0 \sin(\omega_1 t) \quad 0 \leq \phi < \pi \\
&(II)\ v(t) = -A_0 \sin(\omega_2 t) \quad \pi \leq \phi < 2\pi
\end{aligned} \tag{A.3}$$

$$\begin{aligned}
&(I)\ \ i(t) = A_0\sqrt{\frac{C_1}{L}}\cos(\omega_1 t) \quad 0 \leq \phi \leq \pi \\
&(II)\ i(t) = A_0\sqrt{\frac{C_2}{L}}\cos(\omega_2 t) \quad \pi \leq \phi \leq 2\pi
\end{aligned} \tag{A.4}$$

Injecting a current impulse ($i_{INPUT}$ in Figure A.1) of area Δq at time $t_0$ will cause a step voltage change of Δq/C across the capacitor, but cannot instantaneously change the current through the inductor. Equivalently, the voltages' and currents' amplitudes will increased by ΔV, and phases shifted by Δθ. Equating these two sets of equations at $t_0^+$, we get:

$$
\begin{aligned}
&(I)\ \ v(t) = -A_0 \sin(\omega_1 t) + \frac{\Delta q}{C_1} = -(A_0 + \Delta V)\sin(\omega_1 t + \Delta\theta_1) \quad 0 \le \phi < \pi \\
&(II)\ v(t) = -A_0 \sin(\omega_2 t) + \frac{\Delta q}{C_2} = -(A_0 + \Delta V)\sin(\omega_2 t + \Delta\theta_2) \quad \pi \le \phi < 2\pi
\end{aligned}
\tag{A.5}
$$

$$
\begin{aligned}
&(I)\ \ i(t) = A_0\sqrt{\frac{C_1}{L}}\cos(\omega_1 t) = (A_0 + \Delta V)\sqrt{\frac{C_1}{L}}\cos(\omega_1 t + \Delta\theta_1) \quad 0 \le \phi \le \pi \\
&(II)\ i(t) = A_0\sqrt{\frac{C_2}{L}}\cos(\omega_2 t) = (A_0 + \Delta V)\sqrt{\frac{C_2}{L}}\cos(\omega_2 t + \Delta\theta_2) \quad \pi \le \phi \le 2\pi
\end{aligned}
\tag{A.6}
$$

Expanding these terms, and using the small signal equivalencies:

$$
\begin{aligned}
&\cos(\Delta\theta) \approx 1 \\
&\sin(\Delta\theta) \approx \Delta\theta \\
&A_0 + \Delta V \approx A_0
\end{aligned}
\tag{A.7}
$$

we get (voltage equations):

$$
\begin{aligned}
&\frac{\Delta q}{C_1} = -\Delta V \sin(\omega_1 t_0) - A_0 \cdot \Delta\theta_1 \cdot \cos(\omega_1 t_0) \quad 0 \le \phi \le \pi \\
&\frac{\Delta q}{C_2} = -\Delta V \sin(\omega_2 t_0) - A_0 \cdot \Delta\theta_2 \cdot \cos(\omega_2 t_0) \quad \pi \le \phi \le 2\pi
\end{aligned}
\tag{A.8}
$$

and (current equations):

$$
\begin{aligned}
&0 = \Delta V \cos(\omega_1 t_0) - \Delta\theta_1 \cdot A_0 \cdot \sin(\omega_1 t_0) \quad 0 \le \phi \le \pi \\
&0 = \Delta V \cos(\omega_2 t_0) - \Delta\theta_2 \cdot A_0 \cdot \sin(\omega_2 t_0) \quad \pi \le \phi \le 2\pi
\end{aligned}
\tag{A.9}
$$

To compute the phase ISF (Γ), both sides of the voltage equations are multiplied by $\cos(\omega_X t_0)$ and the current equations by $\sin(\omega_X t_0)$, giving (voltage equations):

$$\begin{aligned}
\frac{\Delta q}{C_1}\cos(\omega_1 t_0) &= -\Delta V \cdot \sin(\omega_1 t_0)\cdot\cos(\omega_1 t_0) - A_0 \cdot \Delta\theta_1 \cdot \cos^2(\omega_1 t_0) \qquad 0 \le \phi \le \pi \\
\frac{\Delta q}{C_2}\cos(\omega_2 t_0) &= -\Delta V \cdot \sin(\omega_2 t_0)\cdot\cos(\omega_2 t_0) - A_0 \cdot \Delta\theta_2 \cdot \cos^2(\omega_2 t_0) \qquad \pi \le \phi \le 2\pi
\end{aligned} \tag{A.10}$$

and (current equations):

$$\begin{aligned}
0 &= \Delta V \cdot \sin(\omega_1 t_0)\cdot\cos(\omega_1 t_0) - A_0 \cdot \Delta\theta_1 \cdot \sin^2(\omega_1 t_0) \qquad 0 \le \phi \le \pi \\
0 &= \Delta V \cdot \sin(\omega_2 t_0)\cdot\cos(\omega_2 t_0) - A_0 \cdot \Delta\theta_2 \cdot \sin^2(\omega_2 t_0) \qquad \pi \le \phi \le 2\pi
\end{aligned} \tag{A.11}$$

Substituting the current equations into the voltage equations, and noting that $\cos^2 x + \sin^2 x = 1$, we get:

$$\begin{aligned}
\Delta\theta_1 &= -\frac{\Delta q}{C_1 A_0}\cdot\cos(\omega_1 t_0) \qquad 0 \le \phi \le \pi \\
\Delta\theta_2 &= -\frac{\Delta q}{C_2 A_0}\cdot\cos(\omega_2 t_0) \qquad \pi \le \phi \le 2\pi
\end{aligned} \tag{A.12}$$

Thus, the phase impulse response is (including the capacitance equivalencies of Equation A.2):

$$\begin{aligned}
h_\theta(t,\tau) &= -\frac{\cos(\omega_1\tau)}{q_{MAX}}u(t-\tau) \qquad 0 \le \phi \le \pi \\
h_\theta(t,\tau) &= -\left(\frac{\omega_2}{\omega_1}\right)^2\frac{\cos(\omega_2\tau)}{q_{MAX}}u(t-\tau) \qquad \pi \le \phi \le 2\pi
\end{aligned} \tag{A.13}$$

And, finally, the phase ISF is:

$$\begin{aligned}\Gamma_I(\omega_1 t) &= -\cos(\omega_1 t) && 0 \le \phi \le \pi \\ \Gamma_{II}(\omega_2 t) &= -\left(\frac{\omega_2}{\omega_1}\right)^2 \cos(\omega_2 t) && \pi \le \phi \le 2\pi\end{aligned} \tag{A.14}$$

As is common, the ISF may also be expressed as a function of x, rather than $\omega_1 t$ and $\omega_2 t$, with a simple change of variables. However, in this case, a great deal of intuition is lost by doing so:

$$\begin{aligned}\Gamma(x) &= -\cos\left(\frac{\omega_1+\omega_2}{2\omega_2}\cdot x\right) && 0 \le x \le \frac{\omega_2}{\omega_1+\omega_2}\cdot 2\pi \\ &= -\left(\frac{\omega_2}{\omega_1}\right)^2 \cos\left(\frac{\omega_1+\omega_2}{2\omega_1}\cdot x + \frac{\omega_1-\omega_2}{\omega_1}\cdot \pi\right) && \frac{\omega_2}{\omega_1+\omega_2}\cdot 2\pi \le x \le 2\pi\end{aligned} \tag{A.15}$$

Even without explicitly computing the mean of Γ to produce $\Gamma_{DC}$, it is obvious that the mean of each half function of equation A.14 is zero, for they are cosine functions. In Figure A.2, the piecewise continuous waveform and resultant Γ is plotted for the exaggerated case of $\omega_1/\omega_2=2$. Note that the mean of either half of Γ is zero, due to the half waveforms' odd symmetry about the x-axis.

Thus, the Hajimiri model predicts that no flicker noise is directly upconverted into phase noise. This is perhaps not surprising, given that the waveform was chosen to model AM-FM effects, but does discount the claim that "neglecting AM-to-PM conversion is not a dominant source of error in prediction of phase-noise in integrated electrical oscillators." [17] For this waveform, and insofar as it successfully models them, for integrated LC oscillators, AM-to-PM is the only mechanism which can convert flicker

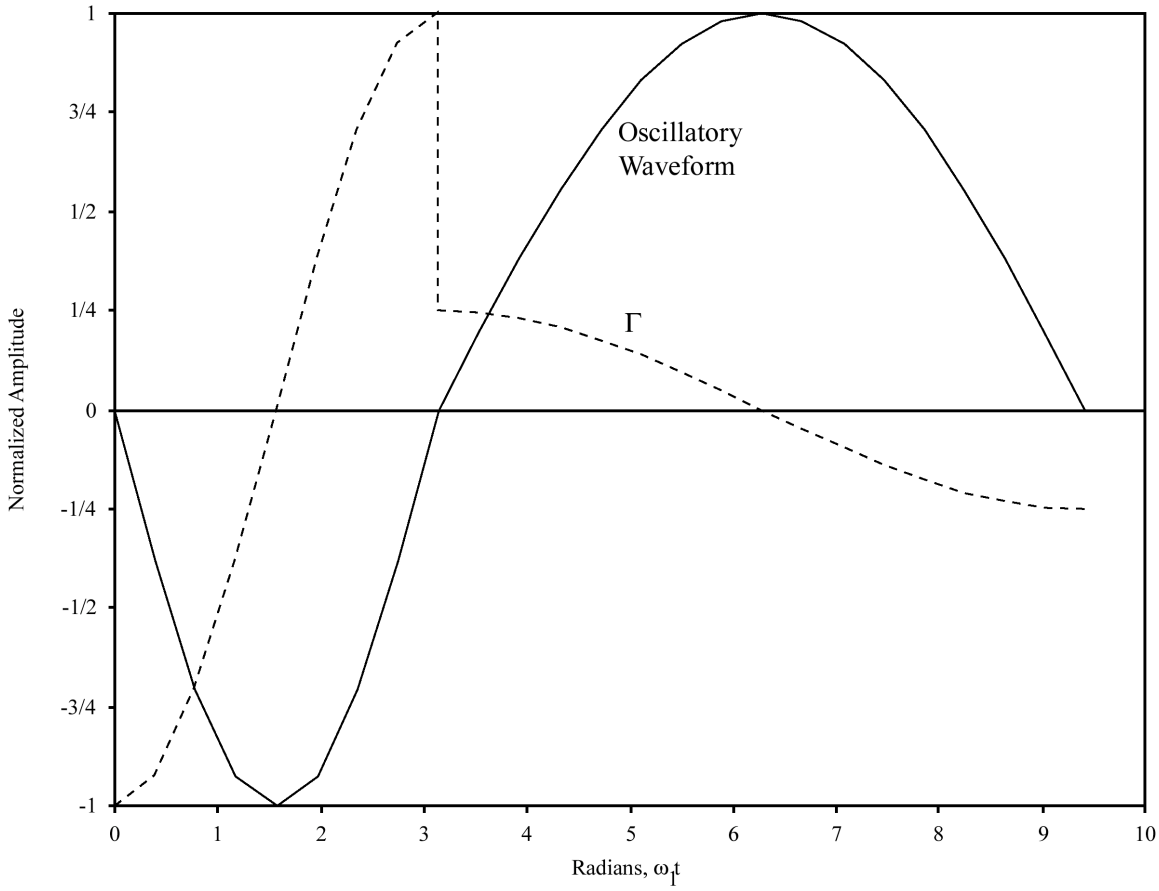



Figure A.2. Piecewise Continuous Oscillatory Waveform and Phase ISF ($\omega_1/\omega_2=2$).

noise into phase noise.

Although not formally proven, the sense given from the above development is that the Hajimiri model can only directly indicate flicker noise upconversion in waveforms with asymmetric rise and fall times, and is thus more suited to ring oscillators, for example, than LC oscillators for flicker noise. Although a more rigorous approach would compute the cross-correlations between the amplitude and phase noises, in addition to the autocorrelations [42], all that is left to do within the Hajimiri context is to compute the Amplitude Impulse Sensitivity Function ($\Lambda$), and to assume a constant proportionate to the AM-to-FM.

The Amplitude Impulse Sensitivity Function may be computed by first multiplying equations A.8 and A.9 by $\sin(\omega_X t_0)$ and $\cos(\omega_X t_0)$, respectively. Doing so, and solving for $\Delta V$, we get:

$$\begin{aligned} \Delta V_1 &= -\frac{\Delta q}{C_1} \cdot \sin(\omega_1 t_0) \qquad 0 \le \phi \le \pi \\ \Delta V_2 &= -\frac{\Delta q}{C_2} \cdot \sin(\omega_2 t_0) \qquad \pi \le \phi \le 2\pi \end{aligned} \tag{A.16}$$

And thus, the Amplitude Impulse Sensitivity functions are:

$$\begin{aligned} \Lambda(\omega_1 t_0) &= -\sin(\omega_1 t_0) \qquad\qquad 0 \le \phi \le \pi \\ \Lambda(\omega_2 t_0) &= -\left(\frac{\omega_2}{\omega_1}\right)^2 \sin(\omega_2 t_0) \quad \pi \le \phi \le 2\pi \end{aligned} \tag{A.17}$$

Being sine functions, each half period will have a non-zero mean value, and the net function will only have a zero mean if the two half periods have equal and opposite means. The mean of each half period may be computed by:

$$\begin{aligned} \bar{f} &= \frac{1}{b-a}\int_a^b f(x)dx \\ \overline{\Lambda}(\omega_1 t) &= \frac{-1}{\pi - 0} \cdot \frac{1}{\omega_1}\int_0^{\pi} \sin(\omega_1 t)(\omega_1 dt) \\ &= -\frac{2}{\pi} \cdot \frac{1}{\omega_1} \end{aligned} \tag{A.18}$$

$$\begin{aligned}\overline{\Lambda}(\omega_2 t) &= \frac{-1}{2\pi-\pi}\cdot\left(\frac{\omega_2^2}{\omega_1^2}\right)\cdot\frac{1}{\omega_2}\int_{\pi}^{2\pi}\sin(\omega_2 t)(\omega_2 dt)\\ &= \frac{2}{\pi}\cdot\frac{\omega_2}{\omega_1^2}\end{aligned} \tag{A.19}$$

$$\Lambda_{DC} = \overline{\Lambda}(\omega_1 t)+\overline{\Lambda}(\omega_2 t) = \frac{2}{\pi}\left(\frac{\omega_2-\omega_1}{\omega_1^2}\right) \tag{A.20}$$

It is interesting to note that the $\Lambda_{DC}$ for the case $C_1=C_2$ (i.e., assuming a step inductor change instead of a step capacitor change) is:

$$\Lambda_{DC}(stepL) = \frac{2}{\pi}\left(\frac{1}{\omega_2}-\frac{1}{\omega_1}\right) \tag{A.21}$$

which is similar to the value detected by the ideal peak detectors of Equation 4.4. This will be used to develop a sense of the error bounds of the $\Lambda_{DC}$ estimate made by peak detectors in Appendix B.

Taking the place of the unit step function in the phase impulse response (Equation A.13) in the amplitude impulse response is the function $d(t-\tau)$, which describes the limiting action of the oscillator [17]. Although the exact amplitude response requires detailed knowledge of the oscillator, most oscillators' amplitude response can be approximated as first or second order, with bandwidth $\omega_0/Q$ [17]. Thus, for the narrow bandwidths of interest to a flicker noise analysis, $d(t-\tau)=1$ is an accurate approximation.

# APPENDIX B

## ERROR OF THE $\Lambda_{DC}$ ESTIMATE DEVELOPED VIA EQUATION 4.4 FOR THE WAVEFORM OF FIGURE 4.2

If the $\Lambda_{DC}$ estimator of Equation 4.4 is used, as in the development of chapter 4, to minimize the flicker noise upconversion, it is not necessary that the estimate be maximally accurate for every $\Lambda_{DC}$ between 0 and 1, but merely that it be maximally accurate near to $\Lambda_{DC}$=0, and for the estimation error to be smooth and monotonic, so that this minima may easily be found by a direct search algorithm. This appendix develops the error expression for the estimator to show that this is so. In the unlikely case that ω1/ω2 is known for a given state in the adaptive oscillator, the error expression could be used to exactly correct the estimate.

If two ideal complementary rectifiers existed, one passing only the signal above the x-axis of Figure 4.2, and the other only the signal below it, the means of the positive and negative rectifier outputs would be:

$$\begin{aligned} \bar{f} &= \frac{1}{b-a}\int_a^b f(x)dx \\ \bar{v}_p &= \frac{-A_0}{\pi-0}\cdot\frac{1}{\omega_1}\int_0^{\pi}\sin(\omega_1 t)(\omega_1 dt) \\ &= -\frac{2A_0}{\pi}\cdot\frac{1}{\omega_1} \\ \bar{v}_n &= \frac{2A_0}{\pi}\cdot\frac{1}{\omega_2} \end{aligned} \tag{B.1}$$

and the mean of the means of the positive and negative peaks is then:

$$\hat{\Lambda}_{DC} = \frac{\bar{v}_p + \bar{v}_n}{2} = \frac{A_0}{\pi}\left[\frac{1}{\omega_2} - \frac{1}{\omega_1}\right] \tag{B.2}$$

Being of similar form to the $\Lambda_{DC}$ estimate of Equation A.20, minimizing the magnitude of the mean of Equation B.2 also minimizes the $\Lambda_{DC}$, and in that sense is a successful estimator of $\Lambda_{DC}$. At $\Lambda_{DC}$=0, the mean of Equation B.2 is also =0, and is thus an exact estimator. Away from 0, there is some error.

If it is assumed that the amplitude of oscillation is known (or can be successfully estimated as Vdd/2-Vsat), then an error as a function of ω1,ω2 can be defined as:

$$\begin{aligned}\varepsilon &= \Lambda_{DC} - \hat{\Lambda}_{DC} \cdot \frac{2}{A_0} \\ &= \frac{2}{\pi}\left(\frac{\omega_2 - \omega_1}{\omega_1^2}\right) - \frac{2}{\pi}\left(\frac{\omega_1 - \omega_2}{\omega_1 \omega_2}\right) \\ &= \frac{2}{\pi}\left[\frac{(\omega_2 - \omega_1)(\omega_2 + \omega_1)}{\omega_1^2 \omega_2}\right]\end{aligned} \tag{B.3}$$

This is plotted versus ω1/ω2 below, as Figure B.1.

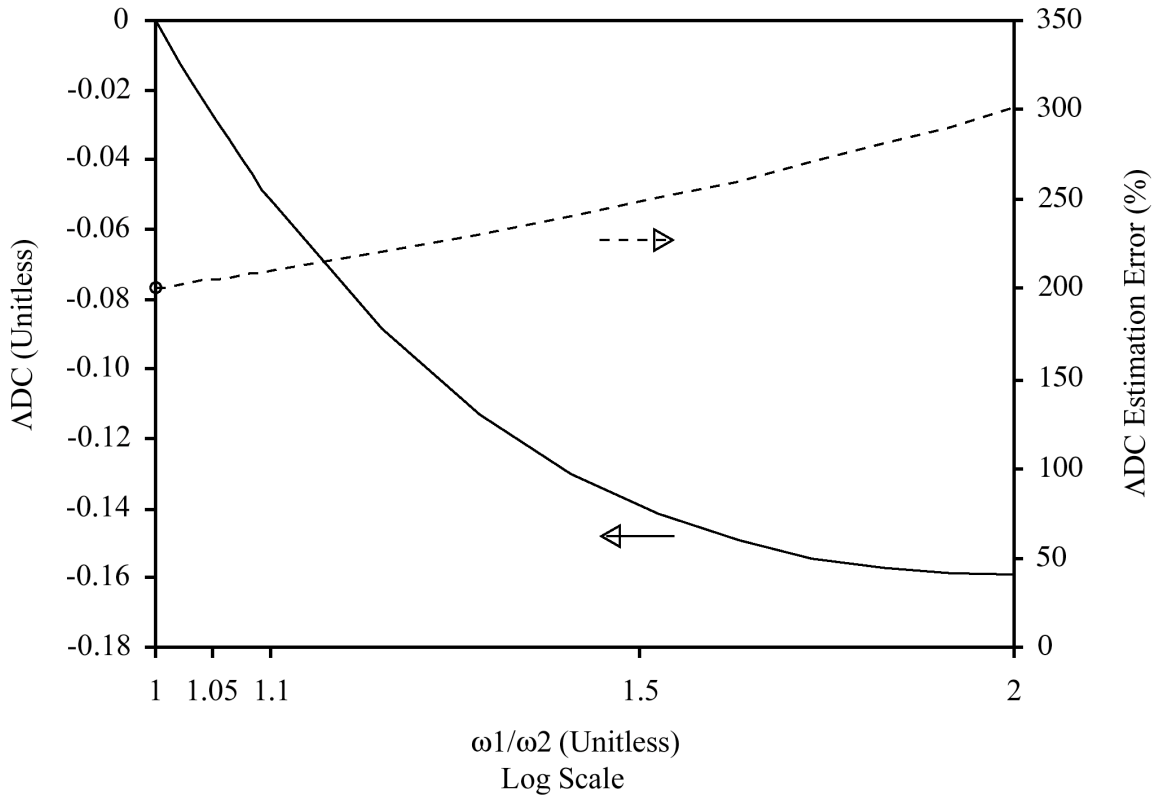



Figure B.1. $\Lambda_{DC}$ and Error of the $\Lambda_{DC}$ Estimate Developed via Equation 4.4 Versus $\omega_1/\omega_2$.

Note that the percentage estimation error is undefined at $\omega_1/\omega_2 = 1$ (and thus $\Lambda_{DC}=0$), as both the estimator and the $\Lambda_{DC}$ equal zero at this point. Thus, the estimate is exact at this point, even though

$$\lim_{\frac{\omega_1}{\omega_2}\to 1+} \frac{\varepsilon}{\Lambda_{DC}} = 200\% \tag{B.4}$$

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